Quad ADC with Diagnostics

Data Sheet

ADAU1977

FEATURES

- Programmable microphone bias (5 V to 9 V) with diagnostics
- Four 10 V rms capable direct-coupled differential inputs
- On-chip PLL for master clock
- Low EMI design
- 106 dB ADC dynamic range
- −95 dB THD + N
- Selectable digital high-pass filter
- 24-bit ADC with 8 kHz to 192 kHz sample rates
- Digital volume control with autoramp function
- I²C/SPI control
- Software-controllable clickless mute
- Software power-down
- Right justified, left justified, I²S justified, and TDM modes
- Master and slave operation modes
- 40-lead LFCSP package
- Qualified for automotive applications

APPLICATIONS

- Automotive audio systems
- Active noise cancellation system

GENERAL DESCRIPTION

The ADAU1977 incorporates four high performance analog-to-digital converters (ADCs) with direct-coupled inputs capable of 10 V rms. The ADC uses multibit sigma-delta (Σ-Δ) architecture with continuous time front end for low EMI. The ADCs can be connected to the electret microphone (ECM) directly and provide the bias for powering the microphone. Built-in diagnostic circuitry detects faults on input lines and includes comprehensive diagnostics for faults on microphone inputs. The faults reported are short to battery, short to microphone bias, short to ground, short between positive and negative input pins, and open input terminals. In addition, each diagnostic fault is available as an IRQ flag for ease in system design. An I²C/SPI control port is also included. The ADAU1977 uses only a single 3.3 V supply. The part internally generates the microphone bias voltage. The microphone bias is programmable in a few steps from 5 V to 9 V. The low power architecture reduces the power consumption. An on-chip PLL can derive the master clock from an external clock input or frame clock (sample rate clock). When fed with a frame clock, the PLL eliminates the need for a separate high frequency master clock in the system. The ADAU1977 is available in a 40-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

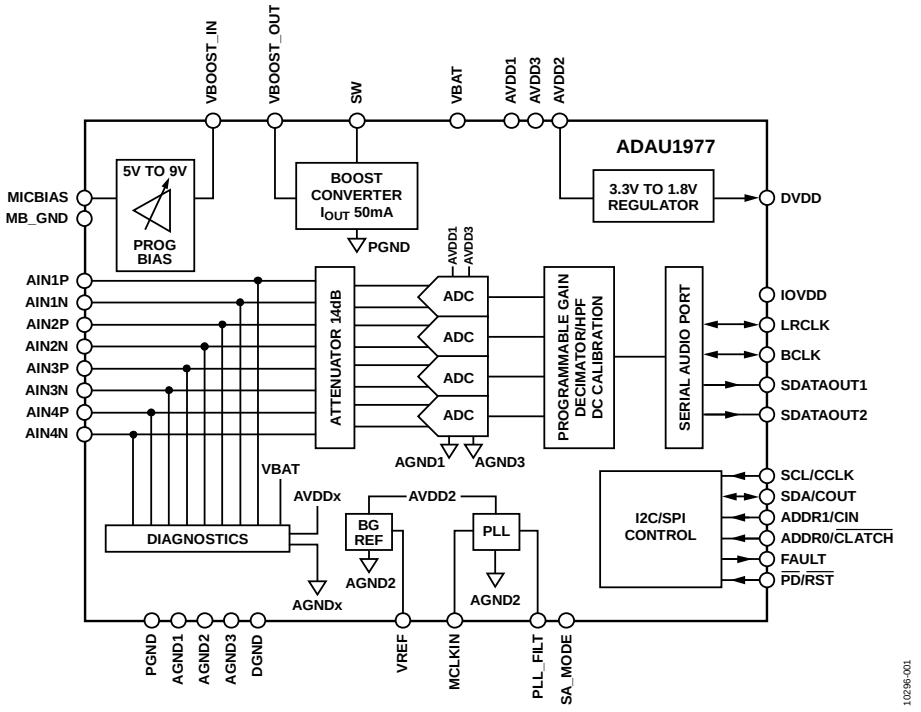

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

1/13—Revision 0: Initial Version

SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. AVDDx/IOVDD = 3.3 V; DVDD (internally generated) = 1.8 V; VBAT = 14.4 V; T_A = −40°C to +105°C, unless otherwise noted; master clock = 12.288 MHz (48 kHz f_S, 256 × f_S mode); input sample rate = 48 kHz; measurement bandwidth = 20 Hz to 20 kHz; word width = 24 bits; load capacitance (digital output) = 20 pF; load current (digital output) = ±1 mA; digital input voltage high = 2.0 V; digital input voltage low = 0.8 V.

ANALOG PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LINE INPUT APPLICATION	See Figure 46				
Full-Scale Differential Input Voltage	DC-coupled, V_{CM} at AINxP/AINxN = 7 V		10		V rms
Full-Scale Single-Ended Input Voltage	DC-coupled, V_{CM} at AINxP/AINxN = 7 V		5		V rms
MICROPHONE INPUT APPLICATION	See Figure 46, MICBIAS = 8.5 V				
Differential Input Voltage	DC-coupled, V_{CM} at AINxP = 5.66 V, AINxN = 2.83 V		2		V rms
QUASI DC INPUT					
Single-Ended Input Voltage			5		V peak
Input Common-Mode Voltage	V_{CM} at AINxP/AINxN pins	0		8	V dc
Peak Input Voltage	V_{CM} + V ac peak at AINxP/AINxN pins	0		14	V
MICROPHONE BIAS					
Output Voltage	Programmable from 5 V to 9 V in steps of 0.5 V; the output voltage is within the specified load regulation	5		9	V
Load Regulation	From no load to maximum load of 25 mA at 5 V	−1	+0.2	+1	%
	From no load to maximum load of 45 mA at 9 V	−1	+0.3	+1	%
Output Current	At MICBIAS = 5 V			25	mA
	At MICBIAS = 9 V			45	mA
Output Noise	20 Hz to 20 kHz, MICBIAS = 5 V		22	32	µV rms
	20 Hz to 20 kHz, MICBIAS = 9 V		35	54	µV rms
Power Supply Rejection Ratio (PSRR)	350 mV rms, 1 kHz ripple on VBOOST_IN at 10 V		60		dB
Interchannel Isolation at MICBIAS Pin	Referred to full scale at 1 kHz		60		dB
Start-Up Time	With C_{LOAD} = 1 nF		40		ms
BOOST CONVERTER					
Input Voltage		2.97	3.3	3.63	V
Input Current	L = 4.7 µH, f_{SW} = 1.536 MHz, MICBIAS = 9 V at 45 mA load		195		mA
	L = 2.2 µH, f_{SW} = 3.072 MHz, MICBIAS = 9 V at 45 mA load		220		mA
Output Current	MICBIAS = 5 V		50		mA
	MICBIAS = 9 V		88		mA
Load Regulation	From no load to maximum load of 50 mA at MICBIAS = 5 V	−1		+1	%
	From no load to maximum load of 88 mA at MICBIAS = 9 V	−1		+1	%
Input Overcurrent Threshold			900		mA peak
Switching Frequency	f_S = 48 kHz L = 2.2 µH		3.072		MHz
	f_S = 48 kHz, L = 4.7 µH		1.536		MHz
External Load Capacitor at VBOOST_OUT Pin		4.7	10	22	µF
ANALOG-TO-DIGITAL CONVERTERS					
Input Resistance					
Differential	Between AINxP and AINxN		50		kΩ
Single-Ended (Rin_{1977})	Between AINxP and AINxN		25		kΩ
ADC Resolution			24		Bits
Dynamic Range (A-Weighted)[1]	Input = 1 kHz, −60 dBFS				
Line Input	Referred to full-scale differential input = 10 V rms	103	106		dB
Microphone Input	Referred to full-scale differential input = 2 V rms		92		dB
Total Harmonic Distortion Plus Noise (THD + N)	Input = 1 kHz, −1 dBFS (0 dBFS = 10 V rms input)		−95	−89	dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Digital Gain Post ADC	Gain step size = 0.375 dB	−35.625		+60	dB
Gain Error		−10		+10	%
Interchannel Gain Mismatch		−0.25		+0.25	dB
Gain Drift			0.6		ppm/°C
Common-Mode Rejection Ratio (CMRR)	1 V rms, 1 kHz		60		dB
	1 V rms, 20 kHz		56		dB
Power Supply Rejection Ratio (PSRR)	100 mV rms, 1 kHz on AVDDx = 3.3 V		70		dB
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
REFERENCE					
Internal Reference Voltage	VREF pin	1.47	1.50	1.54	V
Output Impedance			20		kΩ
ADC SERIAL PORT					
Output Sample Rate		8		192	kHz

[1] For f_S ranging from 44.1 kHz to 192 kHz.

DIAGNOSTIC AND FAULT SPECIFICATIONS

Applicable to differential microphone input using MICBIAS on AINxP and AINxN pins.

Table 2.

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
INPUT VOLTAGE THRESHOLDS FOR FAULT DETECTION[1]					
Hysteresis AINxP or AINxN Shorted to VBAT	SHT_B_TRIP = 10	0.79 × VBAT	0.85 × VBAT	0.86 × VBAT	V
	SHT_B_TRIP = 01	0.84 × VBAT	0.9 × VBAT	0.91 × VBAT	V
	SHT_B_TRIP = 00	0.89 × VBAT	0.95 × VBAT	0.96 × VBAT	V
	SHT_B_TRIP = 11	0.93 × VBAT	0.975 × VBAT	0.99 × VBAT	V
Hysteresis AINxP and AINxN Shorted Together	SHT_T_TRIP = 00	(MICBIAS/2) ± 0.015	(MICBIAS/2) ± 0.035	(MICBIAS/2) ± 0.047	V
	SHT_T_TRIP = 01	(MICBIAS/2) ± 0.001	(MICBIAS/2) ± 0.017	(MICBIAS/2) ± 0.03	V
	SHT_T_TRIP = 10	(MICBIAS/2) ± 0.05	(MICBIAS/2) ± 0.071	(MICBIAS/2) ± 0.08	V
Hysteresis AINxP or AINxN Shorted to Ground	SHT_G_TRIP = 10	0.04 × VREF	0.1 × VREF	0.13 × VREF	V
	SHT_G_TRIP = 01	0.08 × VREF	0.133 × VREF	0.16 × VREF	V
	SHT_G_TRIP = 00	0.12 × VREF	0.2 × VREF	0.22 × VREF	V
	SHT_G_TRIP = 11	0.19 × VREF	0.266 × VREF	0.28 × VREF	V
Hysteresis AINxP Shorted to MICBIAS	SHT_M_TRIP = 10	0.82 × MICBIAS	0.85 × MICBIAS	0.89 × MICBIAS	V
	SHT_M_TRIP = 01	0.87 × MICBIAS	0.9 × MICBIAS	0.94 × MICBIAS	V
	SHT_M_TRIP = 00	0.92 × MICBIAS	0.95 × MICBIAS	1.0 × MICBIAS	V
	SHT_M_TRIP = 11	0.95 × MICBIAS	0.975 × MICBIAS	1.0 × MICBIAS	V
Hysteresis AINxP or AINxN Open Circuit[2]	Refer to the AINxP shorted to MICBIAS and the AINxN shorted to ground specifications for upper and lower thresholds.				
FAULT DURATION	Programmable	10	100	150	ms

[1] The threshold limits are tested with VREF = 1.5 V, MICBIAS = 5 V to 8.5 V, and VBAT = 11 V to 18 V set using an external source. When VBAT ≤ MICBIAS, a short to VBAT cannot be distinguished from a short to MICBIAS, and reporting a short to VBAT fault takes precedence over a short to MICBIAS fault.
[2] The AINxP open terminal fault cannot be distinguished from the AINxN open terminal fault because the voltage at the AINxP and AINxN pins remain at MICBIAS and ground, respectively, when either of these two terminals becomes open circuit.

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Max	Unit
INPUT				
High Level Input Voltage (V_{IH})		0.7 × IOVDD		V
Low Level Input Voltage (V_{IL})			0.3 × IOVDD	V
Input Leakage Current			±10	µA
Input Capacitance			5	pF
OUTPUT				
High Level Output Voltage (V_{OH})	I_{OH} = 1 mA	IOVDD – 0.60		V
Low Level Output Voltage (V_{OL})	I_{OL} = 1 mA		0.4	V

POWER SUPPLY SPECIFICATIONS

L = 4.7 µH, AVDDx = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_S = 48 kHz (master mode), unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DVDD	On-chip LDO	1.62	1.8	1.98	V
AVDDx		3.0	3.3	3.6	V
IOVDD		1.62	3.3	3.6	V
VBAT[1]			14.4	18	V
IOVDD Current	Master clock = 256 f_S				
Normal Operation	f_S = 48 kHz		450		µA
	f_S = 96 kHz		880		µA
	f_S = 192 kHz		1.75		mA
Power-Down	f_S = 48 kHz to 192 kHz		20		µA
AVDDx Current					
Normal Operation	Boost off, 4-channel ADC, DVDD internal		14		mA
	Boost on, 4-channel ADC, DVDD internal		14.5		mA
	Boost off, 4-channel ADC, DVDD external		9.6		mA
	Boost on, 4-channel ADC, DVDD external		10.1		mA
Power-Down			270		µA
Boost Converter Current					
Normal Operation	Boost on, 4-channel ADC, MICBIAS = 8.5 V, no load		34		mA
	Boost on, 4-channel ADC, MICBIAS = 8.5 V, 42 mA		168		mA
Power-Down			180		µA
DVDD Current					
Normal Operation	DVDD external = 1.8 V		4.5		mA
Power-Down			65		µA
VBAT Current	VBAT = 14.4 V				
Normal Operation			575	625	µA
Power-Down			575	625	µA
POWER DISSIPATION					
Normal Operation	Master clock = 256 f_S, 48 kHz				
AVDDx	DVDD internal, MICBIAS = 8.5 V at 42 mA load		265		mW
Power-Down, All Supplies	$\overline{PD}/\overline{RST}$ pin held low		9		mW

[1] When VBAT ≤ MICBIAS, a short to VBAT cannot be distinguished from a short to MICBIAS, and reporting a short to VBAT fault takes precedence over a short to MICBIAS fault.

DIGITAL FILTERS SPECIFICATIONS

Table 5.

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes, typical at f_S = 48 kHz					
Pass Band		0.4375 × f_S		21		kHz
Pass-Band Ripple				±0.015		dB
Transition Band		0.5 × f_S		24		kHz
Stop Band		0.5625 × f_S		27		kHz
Stop-Band Attenuation			79			dB
Group Delay	f_S = 8 kHz to 96 kHz	22.9844/f_S		479		µs
	f_S = 192 kHz			35		µs
HIGH-PASS FILTER	All modes, typical at 48 kHz					
Cutoff Frequency	At −3 dB point			0.9375		Hz
Phase Deviation	At 20 Hz			10		Degrees
Settling Time						
ADC DIGITAL GAIN	All modes		0		60	dB
Gain Step Size				0.375		dB

TIMING SPECIFICATIONS

Table 6.

Parameter	Limit at Min	Limit at Max	Unit	Description
INPUT MASTER CLOCK (MCLK)				
Duty Cycle	40	60	%	MCLKIN duty cycle; MCLKIN at 256 × f_S, 384 × f_S, 512 × f_S, and 768 × f_S
f_{MCLK}	See Table 10		MHz	MCLKIN frequency, PLL in MCLK mode
RESET				
Reset Pulse	15		ns	$\overline{RST}$ low
PLL				
Lock Time		10	ms	
I²C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period of time, the first clock pulse is generated
t_{DS}	100		ns	Data setup time
t_{DH}	0			Data hold time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	1.3		µs	Bus-free time; time between stop and start
t_{SUSTO}	0.6		µs	Setup time for stop condition
SPI PORT				
t_{CCPH}	35		ns	CCLK high
t_{CCPL}	35		ns	CCLK low
f_{CCLK}		10	MHz	CCLK frequency
t_{CDS}	10		ns	CIN setup to CCLK rising
t_{CDH}	10		ns	CIN hold from CCLK rising
t_{CLS}	10		ns	$\overline{CLATCH}$ setup to CCLK rising
t_{CLH}	40		ns	$\overline{CLATCH}$ hold from CCLK rising
t_{CLPH}	10		ns	$\overline{CLATCH}$ high
t_{COE}		30	ns	COUT enable from $\overline{CLATCH}$ falling
t_{COD}		30	ns	COUT delay from CCLK falling
t_{COTS}		30	ns	COUT tristate from $\overline{CLATCH}$ rising
ADC SERIAL PORT				
t_{ABH}	10		ns	BCLK high, slave mode
t_{ABL}	10		ns	BCLK low, slave mode
t_{ALS}	10		ns	LRCLK setup to BCLK rising, slave mode
t_{ALH}	5		ns	LRCLK hold from BCLK rising, slave mode
t_{ABDD}		18	ns	SDATAOUTx delay from BCLK falling

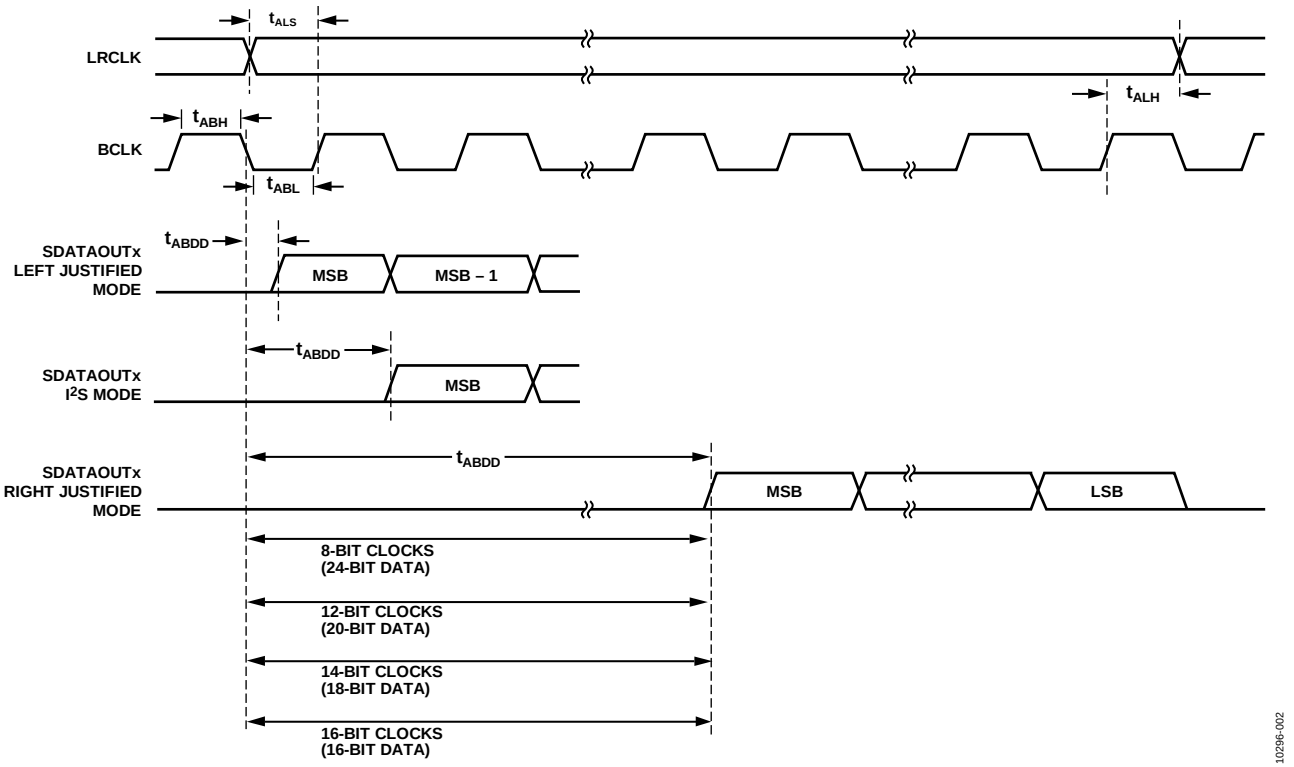


Figure 2. Serial Output Port Timing

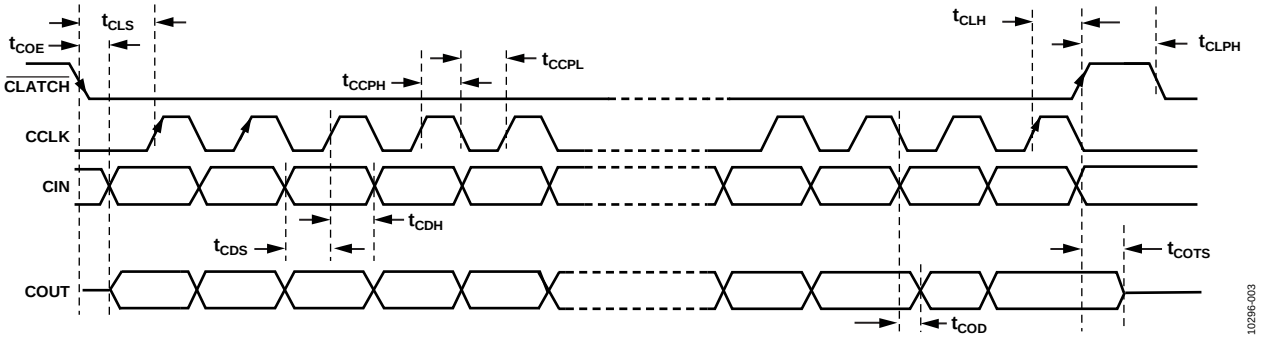


Figure 3. SPI Port Timing

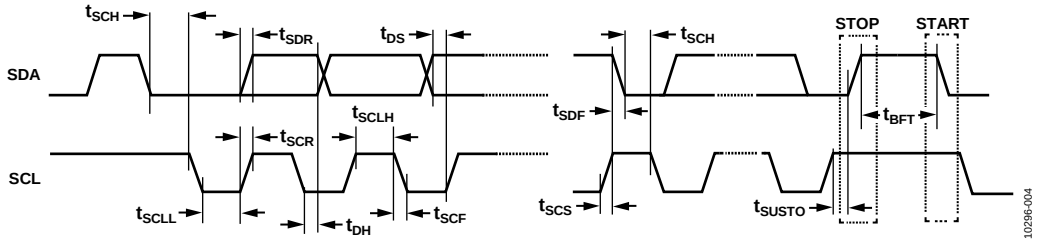


Figure 4. I²C Port Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Analog Supply (AVDDx)	−0.3 V to +3.63 V
Digital Supply	
DVDD	−0.3 V to +1.98 V
IOVDD	−0.3 V to +3.63 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (AINx, VBAT Pins)	−0.3 V to +18 V
Digital Input Voltage (Signal Pins)	−0.3 V to +3.63 V
Operating Temperature Range (Ambient)	−40°C to +105°C
Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} represents junction-to-ambient thermal resistance; θ_{JC} represents the junction-to-case thermal resistance. All characteristics are for a 4-layer JEDEC board.

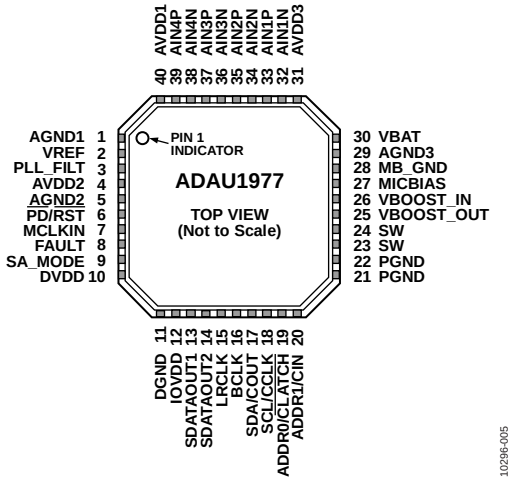
Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	17	2.22	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO THE GROUND PLANE ON THE PCB.

Figure 5. Pin Configuration, 40-Lead LFCSP

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	In/Out[1]	Description
1	AGND1	P	Analog Ground.
2	VREF	O	Voltage Reference. Decouple this pin to AGNDx with 10 µF||100 nF capacitors.
3	PLL_FILT	O	PLL Loop Filter. Return this pin to AVDDx using recommended loop filter components.
4	AVDD2	P	Analog Power Supply. Connect this pin to analog 3.3 V supply.
5	AGND2	P	Analog Ground.
6	$\overline{PD}/\overline{RST}$	I	Power-Down Reset (Active Low).
7	MCLKIN	I	Master Clock Input.
8	FAULT	O	Fault Output. Programmable logic output.
9	SA_MODE	I	Standalone Mode. Connect this pin to IOVDD using a 10 kΩ pull-up resistor for standalone mode.
10	DVDD	O	1.8 V Digital Power Supply Output. Decouple this pin to DGND with a 0.1 µF capacitor.
11	DGND	P	Digital Ground.
12	IOVDD	P	Digital Input and Output Power Supply. Connect this pin to a supply in the range of 1.8 V to 3.3 V.
13	SDATAOUT1	O	ADC Serial Data Output Pair 1.
14	SDATAOUT2	O	ADC Serial Data Output Pair 2.
15	LRCLK	I/O	Frame Clock for the ADC Serial Port.
16	BCLK	I/O	Bit Clock for the ADC Serial Port.
17	SDA/COUT	I/O	Serial Data Output I²C/Control Data Output (SPI).
18	SCL/CCLK	I	Serial Clock Input I²C/Control Clock Input (SPI).
19	ADDR0/$\overline{CLATCH}$	I	Chip Address Bit 0 Setting I²C/Chip Select Input for Control Data (SPI).
20	ADDR1/CIN	I	Chip Address Bit 1 Setting I²C/Control Data Input (SPI).
21	PGND	P	Power Ground Boost Converter.
22	PGND	P	Power Ground Boost Converter.
23	SW	I	Inductor Switching Terminal.
24	SW	I	Inductor Switching Terminal.
25	VBOOST_OUT	O	Boost Converter Output. Decouple this pin to PGND with a 10 µF capacitor.
26	VBOOST_IN	I	MICBIAS Regulator Input. Connect this pin to VBOOST_OUT (Pin 25).
27	MICBIAS	O	Microphone Bias Output. Decouple this pin to AGNDx using a 10 µF capacitor.
28	MB_GND	P	Analog Return Ground for the Microphone Bias Regulator. Connect this pin directly to AGNDx for best noise performance.
29	AGND3	P	Analog Ground.
30	VBAT	I	Voltage Sense for Diagnostics. Connect this pin to a load dump suppressed battery voltage. Decouple this to AGNDx using a 0.1 µF capacitor.

Pin No.	Mnemonic	In/Out[1]	Description
31	AVDD3	P	Analog Power Supply. Connect this pin to an analog 3.3 V supply.
32	AIN1N	I	Analog Input Channel 1 Inverting Input.
33	AIN1P	I	Analog Input Channel 1 Noninverting Input.
34	AIN2N	I	Analog Input Channel 2 Inverting Input.
35	AIN2P	I	Analog Input Channel 2 Noninverting Input.
36	AIN3N	I	Analog Input Channel 3 Inverting Input.
37	AIN3P	I	Analog Input Channel 3 Noninverting Input.
38	AIN4N	I	Analog Input Channel 4 Inverting Input.
39	AIN4P	I	Analog Input Channel 4 Noninverting Input.
40	AVDD1	P	Analog Power Supply. Connect this pin to an analog 3.3 V supply.
	EP		Exposed Pad. The exposed pad must be connected to the ground plane on the printed circuit board (PCB).

[1] I = input, O = output, I/O = input/output, and P= power.

TYPICAL PERFORMANCE CHARACTERISTICS

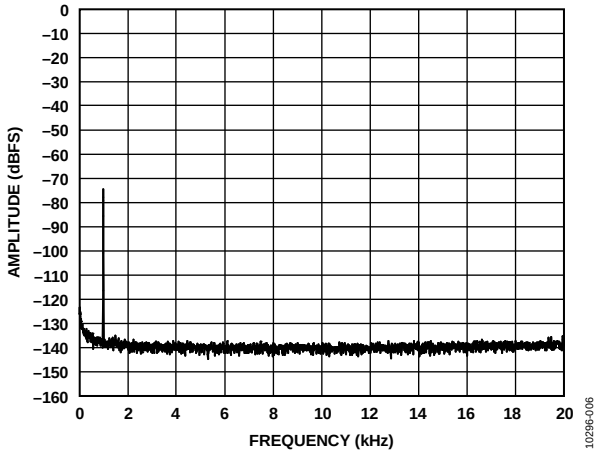


Figure 6. Fast Fourier Transform, 2 mV Differential Input at f_S = 48 kHz

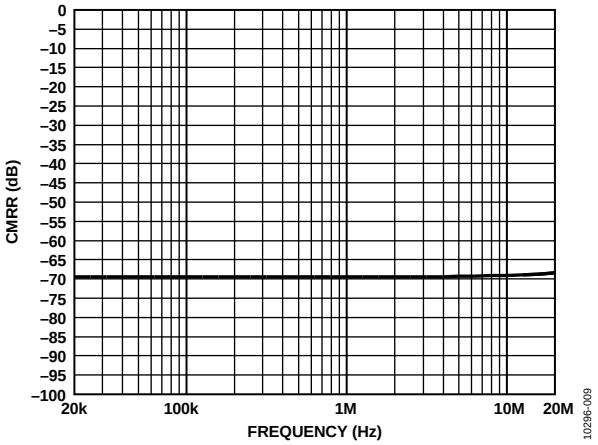


Figure 9. CMRR Differential Input, Referenced to 1 V Differential Input

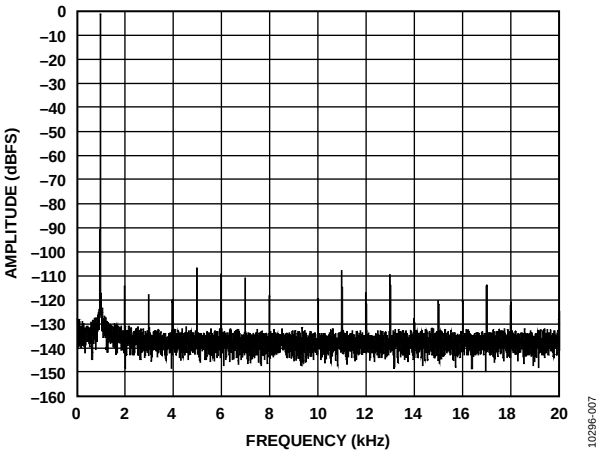


Figure 7. Fast Fourier Transform, −1 dBFS Differential Input

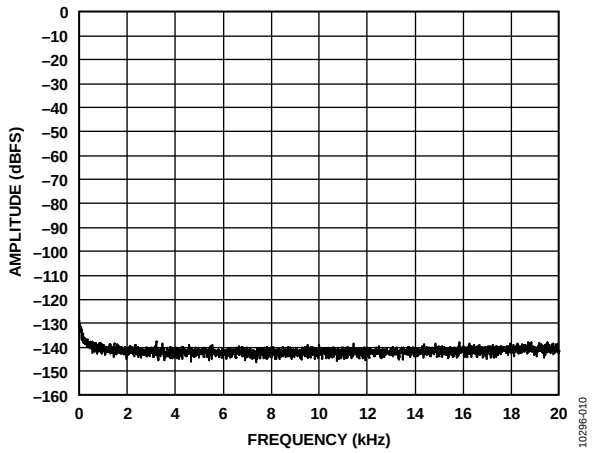


Figure 10. Fast Fourier Transform, No Input

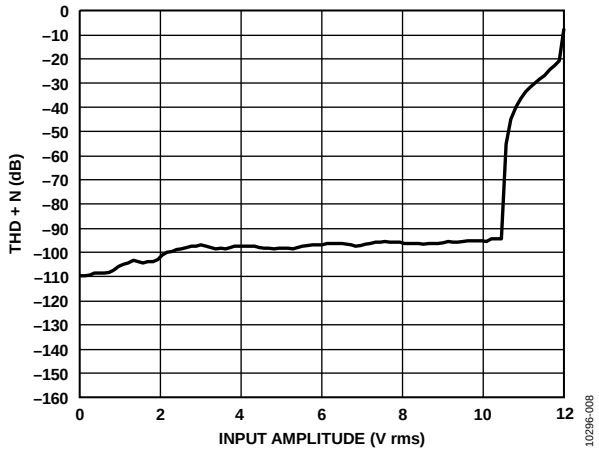


Figure 8. THD + N vs. Input Amplitude

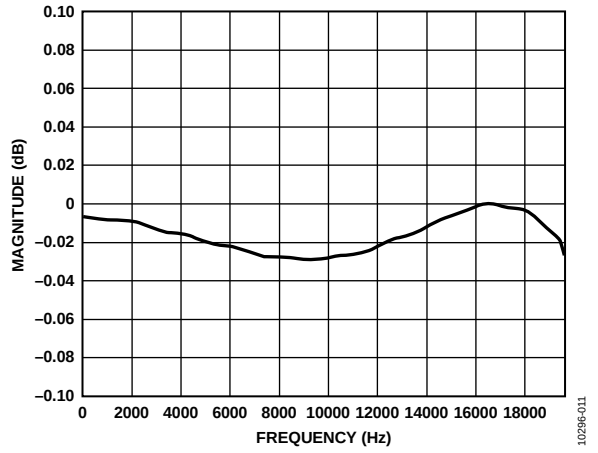


Figure 11. ADC Pass-Band Ripple at f_S = 48 kHz

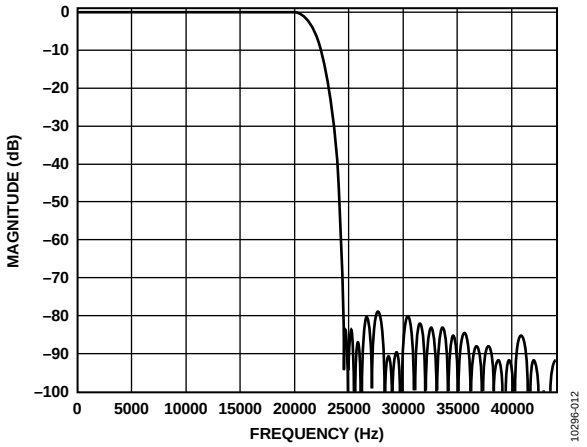


Figure 12. ADC Filter Stop-Band Response at f_S = 48 kHz

THEORY OF OPERATION

OVERVIEW

The ADAU1977 incorporates four high performance ADCs with an integrated boost converter for microphone bias, the associated microphone diagnostics for fault detection, and a phase-locked loop circuit for generating the necessary on-chip clock signals.

POWER SUPPLY AND VOLTAGE REFERENCE

The ADAU1977 requires a single 3.3 V power supply. Separate power supply input pins are provided for the analog and boost converter. These pins should be decoupled to AGND with 100 nF ceramic chip capacitors placed as close as possible to the pins to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 10 µF must be provided on the same PCB as the ADC. It is important that the analog supply be as clean as possible for best performance.

The supply voltage for the digital core (DVDD) is generated using an internal low dropout regulator. The typical DVDD output is 1.8 V and must be decoupled using a 100 nF ceramic capacitor and a 10 µF capacitor. Place the 100 nF ceramic capacitor as close as possible to the DVDD pin.

The voltage reference for the analog blocks is generated internally and output at the VREF pin (Pin 2). The typical voltage at the pin is 1.5 V with an AVDDx of 3.3 V.

All digital inputs are compatible with TTL and CMOS levels. All outputs are driven from the IOVDD supply. The IOVDD can be in the range of 1.8 V to 3.3 V. The IOVDD pin must be decoupled with a 100 nF capacitor placed as close to the IOVDD pin as possible. It is recommended to connect the AGND, DGND, PGND, and exposed pad to a single GND plane on the PCB for best performance.

The ADC internal voltage reference is output from the VREF pin and should be decoupled using a 100 nF ceramic capacitor in parallel with a 10 µF capacitor. The VREF pin has limited current capability. The voltage reference is used as a reference to the ADC; therefore, it is recommended not to draw current from this pin for external circuits. When using this reference, use a noninverting amplifier buffer to provide a reference to other circuits in the application.

In reset mode, the VREF pin is disabled to save power and is enabled only when the $\overline{\text{RST}}$ pin is pulled high.

POWER-ON RESET SEQUENCE

The ADAU1977 requires that a single 3.3 V power supply be provided externally at the AVDDx pin. The part internally generates DVDD (1.8 V), which is used for the digital core of the ADC. The DVDD supply output pin (Pin 10) is provided to connect the decoupling capacitors to DGND. The typical recommended values for the decoupling capacitors are 100 nF in parallel with 10 µF. During a reset, the DVDD regulator is disabled to reduce power consumption. After the $\overline{\text{PD}}/\overline{\text{RST}}$ pin (Pin 6) is pulled high, the part enables the DVDD regulator. However, the internal ADC and digital core reset is controlled by the internal $\overline{\text{POR}}$ signal (power-on reset) circuit, which monitors the DVDD level. Therefore, the device does not come out of a reset until DVDD reaches 1.2 V and the $\overline{\text{POR}}$ signal is released. The DVDD settling time depends on the charge-up time for the external capacitors and on the AVDDx ramp-up time.

The internal POR circuit is provided with hysteresis to ensure that a reset of the part is not initiated by an instantaneous glitch on DVDD. The typical trip points are 1.2 V with $\overline{\text{RST}}$ high and 0.6 V (±20%) with $\overline{\text{RST}}$ low. This ensures that the core is not reset until the DVDD level falls below the 0.6 V trip point.

As soon as the $\overline{\text{PD}}/\overline{\text{RST}}$ pin is pulled high, the internal regulator starts charging up the C_{EXT} on the DVDD pin. The DVDD charge-up time is based on the output resistance of the regulator and the external decoupling capacitor. The time constant can be calculated as

$$t_C = R_{OUT} \times C_{EXT} \ (R_{OUT} = 20\ \Omega \text{ typical})$$

For example, if C_{EXT} is 10 µF, then t_C is 200 µs and is the time to reach the DVDD voltage, within 63.6%.

The POR circuit releases an internal reset of the core when DVDD reaches 1.2 V (see Figure 13). Therefore, it is recommended to wait for at least the t_C period to elapse before sending I²C or SPI control signals.

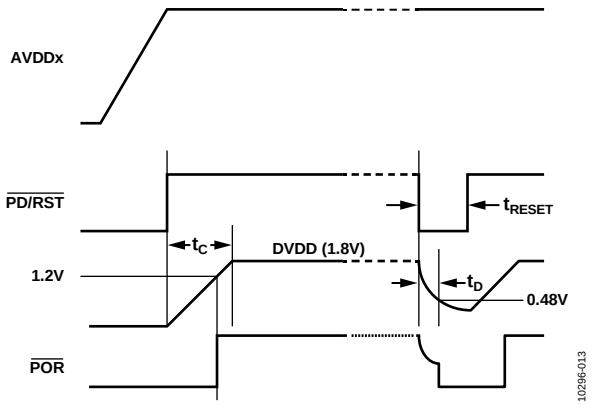


Figure 13. Power-On Reset Timing

When applying a hardware reset to the part by pulling the $\overline{\text{PD}}/\overline{\text{RST}}$ pin (Pin 6) low and then high, there are certain time restrictions. During the $\overline{\text{RST}}$ low pulse period, the DVDD starts discharging. The discharge time constant is decided by the internal resistance of the regulator and C_{EXT}. The time required for DVDD to fall from 1.8 V to 0.48 V (0.6 V − 20%) can be estimated using the following equation:

$$t_D = 1.32 \times R_{INT} \times C_{EXT}$$

where R_{INT} = 64 kΩ typical. (R_{INT} can vary due to process by ±20%.)

For example, if C_{EXT} is 10 µF, then t_D is 0.845 sec.

Depending on C_{EXT}, t_D may vary and in turn decide the minimum hold period for the $\overline{RST}$ pulse. The $\overline{RST}$ pulse must be held low for the t_D time period to initialize the core properly.

The required $\overline{RST}$ low pulse period can be reduced by adding a resistor across C_{EXT}. The new t_D value can then be calculated as

$$t_D = 1.32 \times R_{EQ} \times C_{EXT}$$

where R_{EQ} = 64 kΩ || R_{EXT}.

The resistor ensures that DVDD not only discharges quickly during a reset or an AVDDx power loss but also resets the internal blocks correctly. Note that some power loss in this resistor is to be expected because the resistor constantly draws current from DVDD. The typical value for C_{EXT} is 10 µF and for R_{EXT} is 3 kΩ. This results in a time constant of

$$t_D = 1.32 \times R_{EQ} \times C_{EXT} = 37.8 \text{ ms}$$

where R_{EQ} = 2.866 kΩ (64 kΩ || 3 kΩ).

Using this equation at a set C_{EXT} value, the R_{EXT} can be calculated for a desired $\overline{RST}$ pulse period.

There is also a software reset register (S_RST, Bit 7 of Register 0x00) available that can be used to reset the part, but it must be noted that during an AVDDx power loss, the software reset may not ensure proper initialization because DVDD may not be stable.

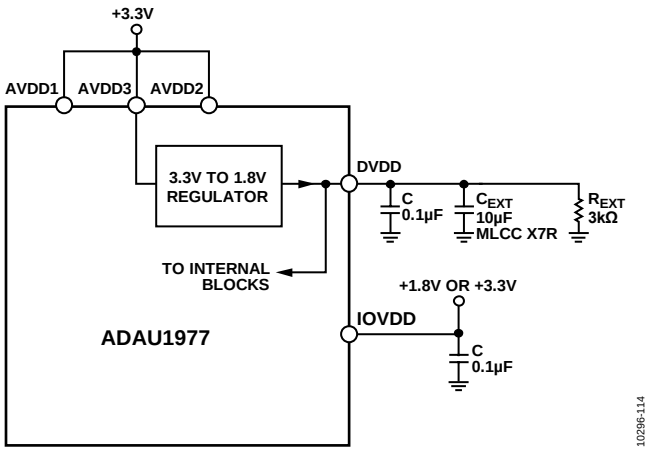


Figure 14. DVDD Regulator Output Connections

PLL AND CLOCK

The ADAU1977 has a built-in analog PLL to provide a jitter-free master clock to the internal ADC. The PLL must be programmed for the appropriate input clock frequency. The PLL Control Register 0x01 is used for setting the PLL.

The CLK_S bit (Bit 4) of Register 0x01 is used for setting the clock source for the PLL. The clock source can be either the MCLKIN pin or the LRCLK pin (slave mode). In LRCLK mode, the PLL can support sample rates between 32 kHz and 192 kHz.

In MCLK input mode, the MCS bits (Bits[2:0] of Register 0x01) must be set to the desired input clock frequency for the MCLKIN pin. Table 10 shows the input MCLK required for the most common sample rates and the MCS bit settings.

The PLL_LOCK bit (Bit 7) of Register 0x01 indicates the lock status of the PLL. It is recommended that after initial power-up the PLL lock status be read to ensure that the PLL outputs the correct frequency before unmuting the audio outputs.

Table 10. Required Input MCLK for Common Sample Rates

MCS (Bits[2:0])	f_S (kHz)	Frequency Multiplication Ratio	MCLKIN Frequency (MHz)
000	32	128 × f_S	4.096
001	32	256 × f_S	8.192
010	32	384 × f_S	12.288
011	32	512 × f_S	16.384
100	32	768 × f_S	24.576
000	44.1	128 × f_S	5.6448
001	44.1	256 × f_S	11.2896
010	44.1	384 × f_S	16.9344
011	44.1	512 × f_S	22.5792
100	44.1	768 × f_S	33.8688
000	48	128 × f_S	6.144
001	48	256 × f_S	12.288
010	48	384 × f_S	18.432
011	48	512 × f_S	24.576
100	48	768 × f_S	36.864
000	96	64 × f_S	6.144
001	96	128 × f_S	12.288
010	96	192 × f_S	18.432
011	96	256 × f_S	24.576
100	96	384 × f_S	36.864
000	192	32 × f_S	6.144
001	192	64 × f_S	12.288
010	192	96 × f_S	18.432
011	192	128 × f_S	24.576
100	192	192 × f_S	36.864

The PLL can accept the audio frame clock (sample rate clock) as input, but the serial port must be configured as a slave and the frame clock must be fed to the part from the master. It is strongly recommended that the PLL be disabled, reprogrammed with the new setting, and then reenabled. A lock bit is provided that can be polled via the I²C to check whether the PLL has acquired lock.

The PLL requires an external filter, which is connected at the PLL_FILT pin (Pin 3). The recommended PLL filter circuit for MCLK or LRCLK mode is shown in Figure 15. Using NPO capacitors is recommended for temperature stability. Place the filter components close to the device for best performance.

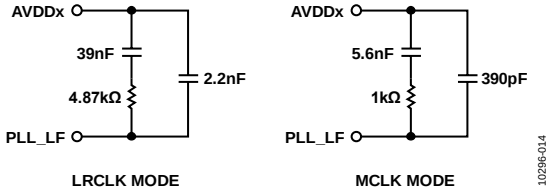


Figure 15. PLL Filter

DC-TO-DC BOOST CONVERTER

The boost converter generates a supply voltage for the microphone bias circuit from a fixed 3.3 V supply. The boost converter output voltage is programmable using Register 0x03. The boost converter output voltage is approximately 1 V above the set microphone bias voltage. The boost converter uses the clock from the PLL, and the switching frequency is dependent on the sample rate of the ADC. The FS_RATE bits (Bits[6:5] of Register 0x02) must be set to the desired sample rate. The boost converter switching frequency can be selected to be 1.5 MHz or 3 MHz using Bit 4 of Register 0x02. For the 1.5 MHz switching frequency, the recommended value for the inductor is 4.7 µH, whereas for the 3 MHz switching frequency, the recommended value for the inductor is 2.2 µH.

Table 12 lists the typical switching frequency based on the sample rates.

Inductor Selection

For the boost converter to operate efficiently, the inductor selection is critical. The two most important parameters for the inductor are the saturation current rating and the dc resistance. The recommended saturation rating for the inductor must be >1 A. The dc resistance affects the efficiency of the boost converter. Assuming that the board trace resistances are negligible for 80% efficiency, the dc resistance of the inductor should be less than 50 mΩ.

Table 11 lists some of the recommended inductors for the application.

Table 11. Recommended Inductors[1]

Value	Manufacturer	Manufacturer Part Number
2.2 µH	Würth Elektronik	7440430022
4.7 µH	Würth Elektronik	7440530047

[1] Check with the manufacturer for the appropriate temperature ratings for a given application.

The boost converter has a soft start feature that prevents inrush current from the input source.

The boost converter has built-in overcurrent and overtemperature protection. The input current to the boost converter is monitored and if it exceeds the set current threshold for 1.2 ms, the boost converter shuts down. The fault condition is recorded into Register 0x02 and asserts the fault interrupt pin. This condition is cleared after reading the BOOST_OV bit (Bit 2) or the BOOST_OC bit (Bit 0) in Register 0x02. The overcurrent protection bit, OC_EN (Bit 1), or the overvoltage protection bit, OV_EN (Bit 3), is on by default, and it is recommended not to disable the bit.

Each protection circuit has two modes for recovery after a fault event: autorecovery and manual recovery. The recovery mode can be selected using Bit 0 of Register 0x03. The autorecovery mode attempts to enable the boost converter after a set recovery time, typically 20 ms. The manual recovery mode enables the boost converter only if the user writes 1 to the MRCV bit (Bit 1). If the fault persists, the boost converter remains in shutdown mode until the fault is cleared.

The boost converter is capable of supplying the 42 mA of total output current at the MICBIAS output. The boost converter has overcurrent protection at the input; the threshold is around 900 mA peak. Ensure that the 3.3 V power supply feeding the boost converter has built-in overcurrent protection because there is no protection internal to ADAU1977 for a short circuit to any of the ground pins (AGND/DGND/PGND) at the VBOOST_OUT or VBOOST_IN pin.

By default, the boost converter is disabled on power-up to allow the flexibility of connecting an external voltage source at the VBOOST_IN pin to power the microphone bias circuit. The boost converter can be enabled by using the BOOST_EN bit (Bit 2 of Register 0x03).

Capacitor Selection

The boost converter output is available at the VBOOST_OUT pin (Pin 25) and must be decoupled to PGND using a 10 µF ceramic capacitor to remove the ripple at the switching frequency. The capacitor must have low ESR and good temperature stability. The MLCC X7R/NPO dielectric type with 25 V is recommended. Care must be taken to place this capacitor as close as possible to the VBOOST_OUT pin (Pin 25).

Table 12. Typical Switching Frequency Based on the Sample Rates

		Boost Converter Switching Frequency	
Base Sample Rate (kHz)	Sample Rates (kHz)	Inductor = 2.2 µH	Inductor = 4.7 µH
32	8/16/32/64	(1024/12) × f_S	(1024/22) × f_S
44.1	11.025/22.05/44.1/88.2/176.4	(1024/16) × f_S	(1024/30) × f_S
48	12/24/48/96/192	(1024/16) × f_S	(1024/32) × f_S

MICROPHONE BIAS

The microphone bias is generated by the input voltage at the VBOOST_IN pin (Pin 26) via a linear regulator to ensure low noise performance and to reject the high frequency noise from the boost converter. If the internal boost converter output is used, the VBOOST_OUT pin (Pin 25) must be connected to the VBOOST_IN pin (Pin 26). If an external supply is used for the microphone bias, the supply can be fed at the VBOOST_IN pin (Pin 26); in this case, leave the VBOOST_OUT pin (Pin 25) open. The microphone bias voltage is programmable from 5 V to 9 V by using the MB_VOLTS bits (Bits[7:4] of Register 0x03). The microphone bias output voltage is available at the MICBIAS pin (Pin 27). This pin can be decoupled to AGND using a maximum of up to a 10 µF capacitor with an ESR of at least 1 Ω. For higher value capacitors, especially those above 1 nF, the ESR of the capacitor should be ≥ 1 Ω to ensure the stability of the microphone bias regulator. Register 0x03 can be used to enable the microphone bias. Table 12 lists the switching frequency of the boost converter based on the inductor value and common sample rates.

ANALOG INPUTS

The ADAU1977 has four differential analog inputs. The ADCs can accommodate both dc- and ac-coupled input signals.

The block diagram shown in Figure 16 represents the typical input circuit.

In most audio applications, the dc content of the signal is removed by using a coupling capacitor. However, the ADAU1977 consists of a unique input structure that allows direct coupling of the input signal, eliminating the need for using a large coupling capacitor at the input. Each input has a fixed 14 dB attenuator connected to AGND for accommodating a 10 V rms differential input. The typical input resistance is approximately 26 kΩ from each input to AGND.

In dc-coupled applications, if the V_{CM} at AINxP and AINxN is the same, the dc content in the ADC output is close to 0. If the input pins are presented with different common-mode dc levels, the difference between the two levels appears at the ADC output and can be removed by enabling the high-pass filter.

The high-pass filter has a 1.4 Hz, 6 dB per octave cutoff at a 48 kHz sample rate. The cutoff frequency scales directly with the sample frequency. However, care is required in dc-coupled applications to ensure that the common-mode dc voltage does not exceed the specified limit. The common-mode loop can accommodate a common-mode dc voltage from 0 V to 7 V. The input required for the full-scale ADC output (0 dBFS) is typically 10 V rms differential.

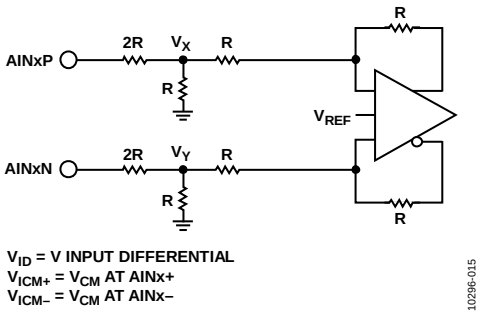


Figure 16. Analog Input Block

Line Inputs

This section describes some of the possible ways to connect the ADAU1977 for line level inputs.

Line Input Balanced or Differential Input DC-Coupled Case

For example, in the case of a typical power amplifier for an automobile, the output can swing around 10 V rms differential with approximately 7.2 V common-mode dc input voltage (assuming a 14.4 V battery and bridge-tied load connection). The signal at each input pin has a 5 V rms or 14.14 V p-p signal swing. With a common-mode dc voltage of 7.2 V, the signal can swing between (7.2 V + 7.07 V) = +14.27 V p-p and (7 V − 7.07 V) = 0.13 V at each input. Therefore, this results in approximately a 28.54 V p-p differential signal swing and measures around −0.16 dBFS (ac only with dc high-pass filter) at the ADC output. See Figure 17.

Line Input Balanced or Differential Input AC-Coupled Case

For an amplifier output case with ac coupling, refer to Figure 18 for information about connecting the line level inputs to the ADAU1977. In this case, the AINxP/AINxN pins must be pulled up to the required common-mode level using the resistors on MICBIAS. The V_{CM} must be such that the input never swings below a ground. In other words, if the input signal is 14 V p-p, the V_{CM} must be around 14 V/2 = 7 V to ensure that the signal never swings below a ground. The microphone bias can provide the required clean reference for generating the V_{CM}.

The R1 value can be calculated as follows:

$$R1 = Rin_{1977}\,(MB - V_{CM})/V_{CM}$$

where:
V_{CM} is the peak-to-peak input swing divided by 2.
MB = 8.5 V.
Rin_{1977} is the single-ended input resistance (see Table 1).

However, in this case the equivalent input resistance of AINxP/AINxN is reduced and can be calculated as R1 || Rin_{1977}.

$$Input\ Resistance = R1 \times Rin_{1977}/(R1 + Rin_{1977})$$

where Rin_{1977} is the single-ended value from Table 1.

The C1 and C2 values can be determined for the required low frequency cutoff using the following equation:

$$C1 \text{ or } C2 = 1/(2 \times \pi \times f_C \times Input\ Resistance)$$

Line Input Unbalanced or Single-Ended Pseudo Differential AC-Coupled Case

For a single-ended application, the signal swing is reduced by half because only one input is used for the signal, and the other input is connected to 0 V. As a result, the input signal capability is reduced to 5 V rms in a single-ended application. With a common-mode dc voltage of 7.2 V, the signal can swing between (7.2 V + 7.07 V) = +14.27 V p-p and (7.2 V − 7 V) = 0.13 V. Therefore, this results in approximately a 14.14 V p-p differential signal swing and measures around −6.16 dBFS (ac only with dc high-pass filter) at the ADC output. See Figure 19.

The values of the resistors (R1/R2) and capacitors (C1/C2) are similar to those for the balanced ac-coupled case described in the Line Input Balanced or Differential Input AC-Coupled Case section.

Line Input Unbalanced or Single-Ended AC-Coupled Case

For a single-ended application, the signal swing is reduced by half because only one input is used for the signal, and the other input is connected to 0 V. As a result, the input signal capability is reduced to 5 V rms in a single-ended application. With a common-mode dc voltage of 7.2 V, the signal can swing between (7.2 V + 7.07 V) = +14.27 V p-p and (7.2 V − 7 V) = 0.13 V. Therefore, this results in approximately a 14.14 V p-p differential signal swing and measures around −6.16 dBFS (ac only with dc high-pass filter) at the ADC output. The difference in the common-mode dc voltage between the positive and negative input (7.2 V) would appear at the ADC output if the signal was not high-pass filtered. See Figure 20.

The values of the resistor (R1) and capacitor (C1) are similar to those for the balanced ac-coupled case described in the Line Input Balanced or Differential Input AC-Coupled Case section.

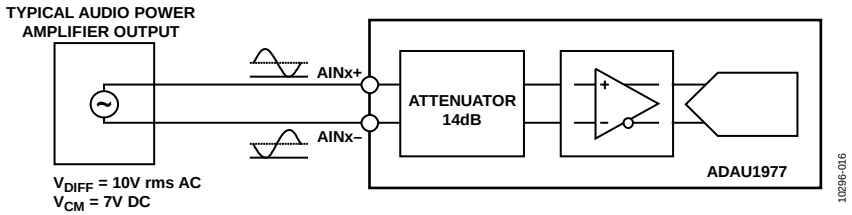


Figure 17. Connecting the Line Level Inputs—Differential DC-Coupled Case

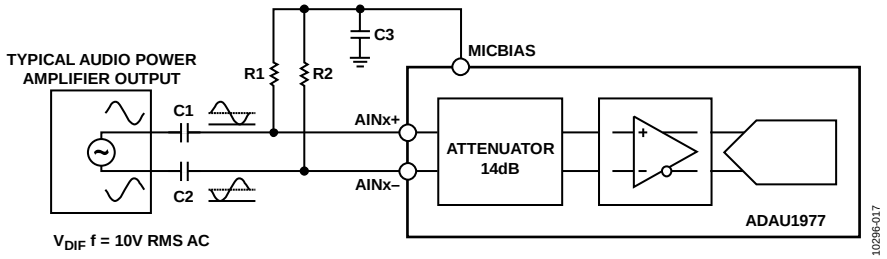


Figure 18. Connecting the Line Level Inputs—Differential AC-Coupled Case

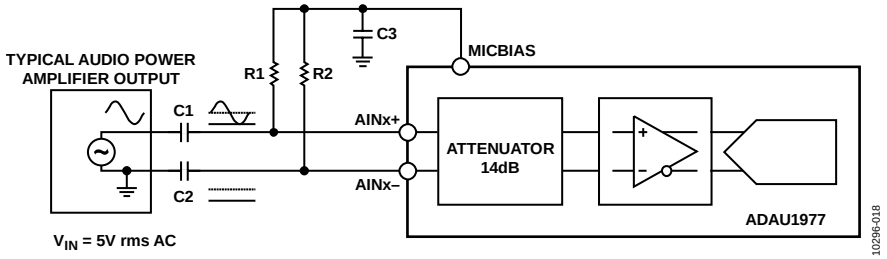


Figure 19. Connecting the Line Level Inputs—Pseudo Differential AC-Coupled Case

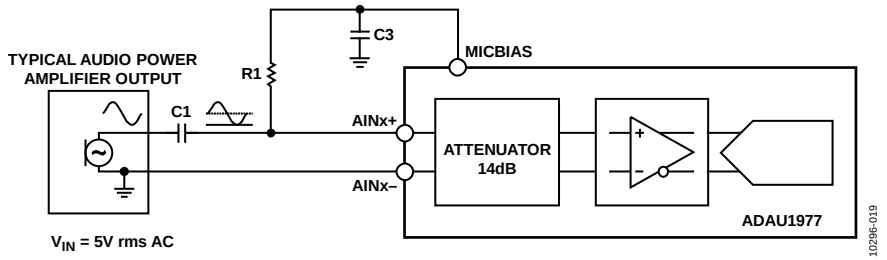


Figure 20. Connecting the Line Level Inputs—Single-Ended AC-Coupled Case

Microphone Inputs

This section describes some ways to connect the ADAU1977 for microphone input applications. The MICBIAS voltage and the bias resistor value depend on the ECM selected. The ADAU1977 can provide the MICBIAS from 5 V up to 9 V in 0.5 V steps. In an application requiring multiple microphones, care must be taken not to exceed the MICBIAS output current rating.

ECM Balanced or Differential Input DC-Coupled Case

For example, in a typical ECM, the output signal swing depends on the MICBIAS voltage. With a typical 8.5 V supply, the ECM can output a 2 V rms differential signal. The signal at each input pin has a 1 V rms or 2.8 V p-p signal swing. With a common-mode dc level of 2/3 × MICBIAS on the AINxP and 1/3 × MICBIAS on the AINxN pins, this results in around −14 dBFS (ac only with dc high-pass filter) at the ADC output because the input is 14 dB below the full-scale input of 10 V rms differential. See Figure 21.

ECM Pseudo Differential Input AC-Coupled Case

For a typical MEMS ECM module, the output signal swing is low. With a typical 3.3 V supply, the ECM module can output a 2 V rms differential signal. The signal at the input pin has a 1 V rms or 2.8 V p-p signal swing. For this application, it is recommended to bias the input pins using resistors to 7 V dc, similar to the case described in the Line Input Unbalanced or Single-Ended Pseudo Differential AC-Coupled Case section. See Figure 22.

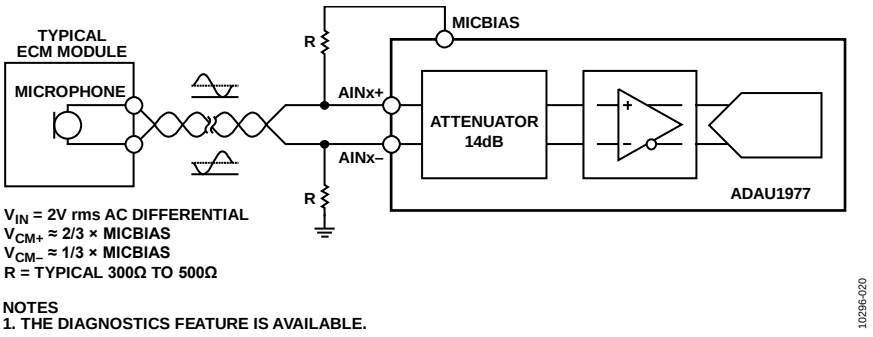


Figure 21. Connecting the Microphone Inputs—Differential Input DC-Coupled Case

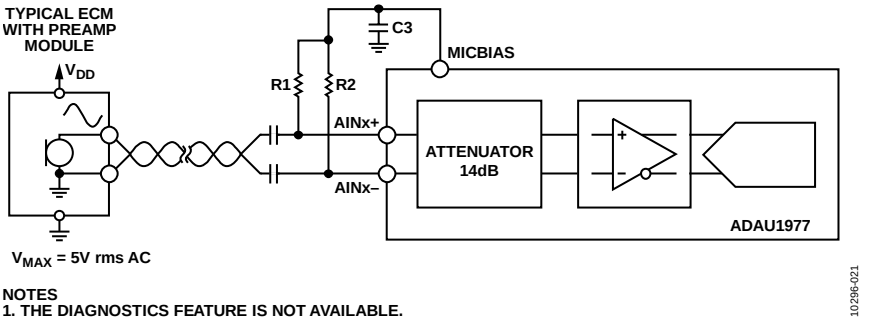


Figure 22. Connecting the Microphone Inputs—Pseudo Differential Input AC-Coupled Case

ADC

The ADAU1977 contains four Δ-Σ ADC channels configured as two stereo pairs with configurable differential/single-ended inputs. The ADC can operate at a nominal sample rate of 32 kHz up to 192 kHz. The ADCs include on-board digital antialiasing filters with 79 dB stop-band attenuation and linear phase response. Digital outputs are supplied through two serial data output pins (one for each stereo pair) and a common frame clock (LRCLK) and bit clock (BCLK). Alternatively, one of the TDM modes can be used to support up to 16 channels on a single TDM data line.

With smaller amplitude input signals, a 10-bit programmable digital gain compensation for an individual channel is provided to scale up the output word to full scale. Care must be taken to avoid overcompensation (large gain compensation), which leads to clipping and THD degradation in the ADC.

The ADCs also have a dc-offset calibration algorithm to null the systematic dc offset of the ADC. This feature is useful for dc measurement applications.

ADC SUMMING MODES

The four ADCs can be grouped into either a single stereo ADC or a single mono ADC to increase the signal-to-noise ratio (SNR) for the application. Two options are available: one option for summing two channels of the ADC and another option for summing all four channels of the ADC. Summing is performed in the digital block.

2-Channel Summing Mode

When the SUM_MODE Bits (Bits[7:6] of Register 0x0E) are set to 01, the Channel 1 and Channel 2 ADC data are combined and output from the SDATAOUT1 pin. Similarly, the Channel 3 and Channel 4 ADC data are combined and output from the SDATAOUT2 pin. As a result, the SNR improves by 3 dB. For this mode, both Channel 1 and Channel 2 must be connected to the same input signal source. Similarly, Channel 3 and Channel 4 must be connected to the same input signal source.

4-Channel Summing Mode

When the SUM_MODE Bits (Bits[7:6] of Register 0x0E) are set to 10, the Channel 1 through Channel 4 ADC data are combined and output from the SDATAOUT1 pin. As a result, the SNR improves by 6 dB. For this mode, all four channels must be connected to the same input signal source.

DIAGNOSTICS

The diagnostics block monitors the input pins in real time and reports a fault as an interrupt signal on the FAULT pin (Pin 8), which triggers sending an interrupt request to an external controller. The diagnostics status registers (Register 0x11 through Register 0x14) for Channel 1 through Channel 4 are also updated. Refer to the register map table (Table 25) and the register details tables (Table 42, Table 43, Table 44, and Table 45) for more information about the diagnostics register content. The diagnostics can be enabled or disabled for each channel using Bits[3:0] of Register 0x10. The diagnostics are provided only when MICBIAS is enabled and the microphone is connected as recommended in the appropriate application circuit (see Figure 21).

Diagnostics Reporting

The diagnostics status is reported individually for each channel in Register 0x11 through Register 0x14. The faults listed in Table 13 are reported on each input pin.

Table 13. Faults Reported

Fault	AINxP	AINxN
Short to Battery	Yes	Yes
Short to MICBIAS	Yes	No
Short to Ground	Yes	Yes
Short Between Positive and Negative Inputs	Yes	Yes
Open Input	Yes	Yes

Diagnostics Adjustments

Short Circuit to Battery Supply

When an input terminal is shorted to the battery, the voltage at the terminal approaches the battery voltage. Any voltage higher than the set threshold is reported as a fault. The threshold can be set using the SHT_B_TRIP bits, Bits[1:0] of Register 0x17 (see Table 14).

Table 14. Setting the Short to Battery Threshold

SHT_B_TRIP (Register 0x17, Bits[1:0])	Short to Battery Threshold
00	0.95 × VBAT
01	0.9 × VBAT
10	0.85 × VBAT
11	0.975 × VBAT

Short Circuit to MICBIAS

This feature is supported only on the AINxP terminal. When an AINxP terminal is shorted to MICBIAS, the voltage at the AINxP terminal approaches the MICBIAS voltage. Any voltage higher than the set threshold is reported as a fault. The threshold can be set using the SHT_M_TRIP bits, Bits[5:4] of Register 0x17 (see Table 15).

Table 15. Setting the Short to MICBIAS Threshold

SHT_M_TRIP (Register 0x17, Bits[5:4])	Short to MICBIAS Threshold
00	0.95 × MICBIAS
01	0.9 × MICBIAS
10	0.85 × MICBIAS
11	0.975 × MICBIAS

Short Circuit to Ground

When an input terminal is shorted to ground, the terminal voltage reaches close to 0 V. Any voltage lower than the set threshold is reported as a fault. The threshold is referenced to VREF and, therefore, scales with the voltage at the VREF pin.

The threshold can be set using the SHT_G_TRIP bits, Bits[3:2] of Register 0x17 (see Table 16).

Table 16.

SHT_G_TRIP (Register 0x17, Bits[3:2])	Short to Ground Threshold
00	0.2 × VREF
01	0.133 × VREF
10	0.1 × VREF
11	0.266 × VREF

Microphone Terminal Short Circuited

When both input terminals are shorted, both the AINxP and AINxN input terminals are at the same voltage—around MICBIAS/2. Any voltage between the set thresholds is reported as a fault. The upper and lower threshold voltages can be set using the SHT_T_TRIP bits, Bits[7:6] of Register 0x17 (see Table 17).

The following equations can be used to calculate the upper and lower thresholds:

$$Upper\ Threshold = MICBIAS(0.5 + x)$$

$$Lower\ Threshold = MICBIAS(0.5 - x)$$

where x can be set using the SHT_T_TRIP bits, Bits[7:6] of Register 0x17 (see Table 17).

Table 17.

SHT_T_TRIP (Register 0x17, Bits [7:6])	x
00	0.035
01	0.017
10	0.071
11	Reserved

Microphone Terminals Open

In the event that any of the input terminals becomes open circuited, AINxP is pulled to MICBIAS and AINxN is pulled to a common ground. When the AINxP terminal is at a voltage that is higher than the short to the MICBIAS threshold (set using Bits[5:4] of Register 0x17) and the AINxN terminal voltage is at a voltage that is less than the short to the ground threshold (set using Bits[3:2] of Register 0x17), a fault is reported. The fault cannot indicate which terminal is open circuited because any terminal that is open circuited pulls AINxP to MICBIAS and AINxN to a common ground.

FAULT Pin

The FAULT pin is an output pin that can be programmed to be active high or active low logic using the IRQ_POL bit (Bit 4 of Register 0x15). In addition, the FAULT pin can be set using the IRQ_DRIVE bit (Bit 5 of Register 0x15) to drive always or to drive only during a fault and is otherwise set to high-Z. The fault status is registered in the IRQ_RESET bit (Bit 6 of Register 0x15). The IRQ_RESET bit is a latched bit and is set in the event of a fault and cleared only after the fault status bit is read.

Fault Timeout

To prevent the false triggering of a fault event, the fault timeout adjust bits (Bits[5:4] of Register 0x18) are provided. These bits can be used to set the time that the fault needs to persist before being reported. The timeout can be set to 0 ms, 50 ms, 100 ms, or 150 ms using the FAULT_TO bits (Bits[5:4] of Register 0x18). The default value is 100 ms. A fault is recorded only if the condition persists for more than a set minimum timeout.

Fault Masking

The faults can be masked to prevent triggering an interrupt on the FAULT pin. Fault masking can be set using Bits[6:0] of Register 0x16. The mask can be set for the faults listed in Table 18.

Table 18. Fault Masking

Fault	AINxP	AINxN
Short to Battery	Yes	Yes
Short to MICBIAS	Yes	No
Short to Ground	Yes	Yes
Short Between Positive and Negative Inputs	Yes	Yes
Open Input	Yes	Yes

When a fault mask bit is set, it is applied to all the channels. There is no individual fault mask available per channel using this bit. To mask individual channels, use the DIAG_MASK[4:1] bits (Bits[3:0] of Register 0x15).

Diagnostics Sequence

The sequence shown in Figure 23 is recommended for reading the faults reported by diagnostics.

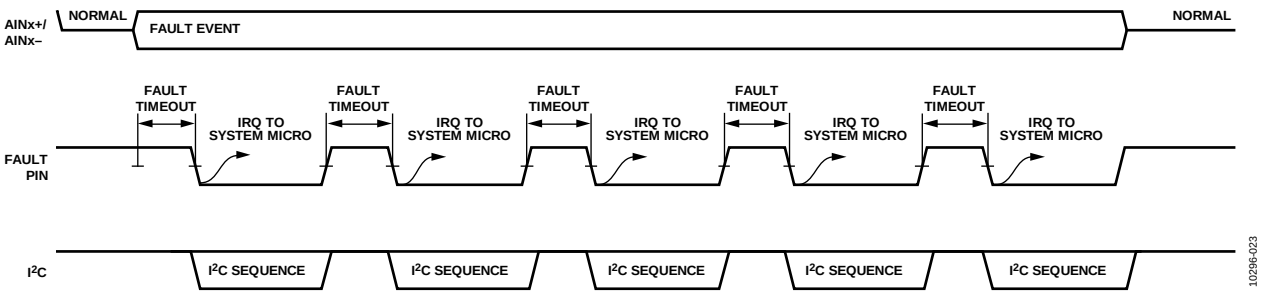


Figure 23. Diagnostics Sequence

In the event of a fault on an input pin, the FAULT pin goes low or high depending on the setting of the IRQ_POL bit in Register 0x15 to send an interrupt request to the system microcontroller. The system microcontroller responds to the interrupt request by communicating with the ADAU1977 via the I²C.

The following is the typical interrupt service routine:

1. An interrupt request is generated from the ADAU1977 to the system microcontroller.
2. Read Register 0x11 through Register 0x14. (It is recommended to read all four diagnostics status registers—Register 0x11 through Register 0x14—in one sequence. Reading the registers as a single read may not report the status accurately.)
3. Write Register 0x15, Bit 6 (the IRQ_RESET bit).
4. Wait for the fault timeout period to expire.
5. If the fault was temporary and did not persist, the interrupt service ends and the intermittent fault is ignored. If the fault persists, another interrupt request is generated from the ADAU1977, and the user should continue on to Step 6.
6. Repeat Step 2 through Step 4 four times.
7. If after the fifth reading, the diagnostics still report the presence of a fault, the fault exists on the respective input and must be attended to.

SERIAL AUDIO DATA OUTPUT PORTS—DATA FORMAT

The serial audio port comprises four pins: BCLK, LRCLK, SDATAOUT1, and SDATAOUT2. The ADAU1977 ADC outputs are available on the SDATAOUT1 and SDATAOUT2 pins in serial format. The BCLK and LRCLK pins serve as the bit clock and frame clock, respectively. The port can be operated as master or slave and can be set either in stereo mode (2-channel mode) or in TDM multichannel mode. The supported popular audio formats are I²S, left justified (LJ), right justified (RJ).

Stereo Mode

In 2-channel or stereo mode, the SDATAOUT1 outputs ADC data for Channel 1 and Channel 2, and the SDATOUT2 outputs ADC data for Channel 3 and Channel 4. Figure 24 through Figure 28 show the supported audio formats.

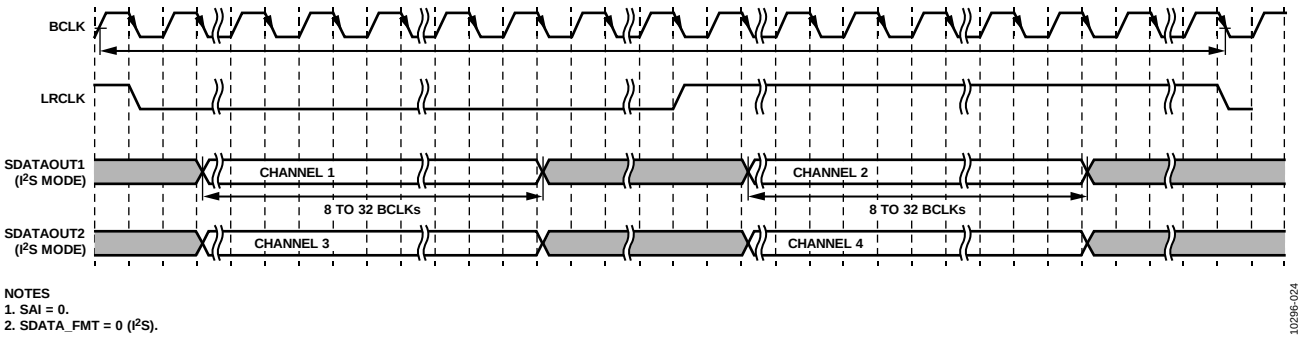


Figure 24. I²S Audio Format

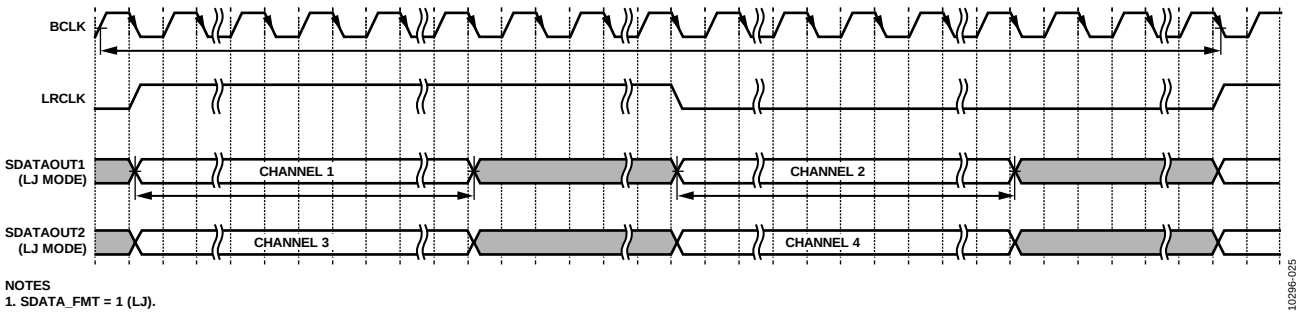


Figure 25. LJ Audio Format

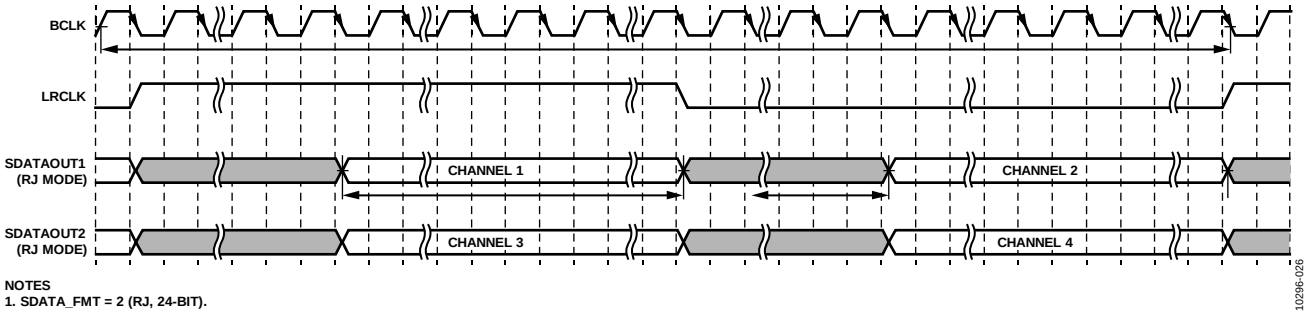


Figure 26. RJ Audio Format

TDM Mode

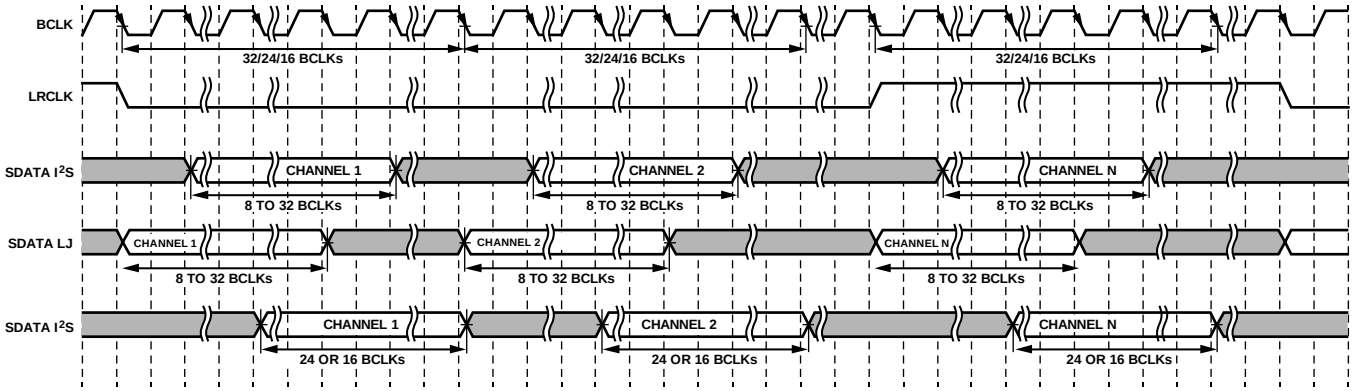
Register 0x05 through Register 0x08 provide programmability for the TDM mode. The TDM slot width, data width, and channel assignment, as well as the pin used to output the data, are programmable.

By default, serial data is output on the SDATAOUT1 pin; however, the SDATA_SEL bit (Bit 7 of Register 0x06) can be used to change the setting so that serial data is output from the SDATAOUT2 pin.

The TDM mode supports 2, 4, 8, or 16 channels. The ADAU1977 outputs four channels of data in the assigned slots (Figure 29 shows the data slot assignments). During the unused slots, the output pin goes high-Z so that the same data line can be shared with other devices on the TDM bus.

The TDM port can be operated as either a master or a slave. In master mode, the BCLK and LRCLK are output from the ADAU1977, whereas in slave mode, the BCLK and LRCLK pins are set to receive the clock from the master in the system.

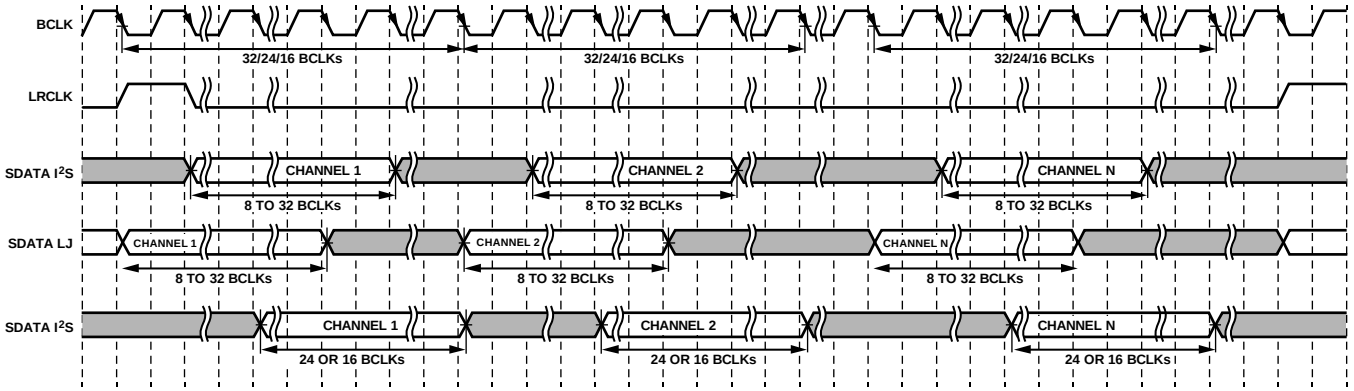
Both the nonpulse and pulse modes are supported. In nonpulse mode, the LRCLK signal is typically 50% of the duty cycle, whereas in pulse mode, the LRCLK signal must be at least one BCLK wide (see Figure 27 and Figure 28).



NOTES
1. SAI = 001 (2 CHANNELS), 010 (4 CHANNELS), 011 (8 CHANNELS), 100 (16 CHANNELS).
2. SDATA_FMT = 00 (I²S), 01 (LJ), 10 (RJ, 24-BIT), 11 (RJ, 16-BIT).
3. BCLK_EDGE = 0.
4. LRCLK_MODE = 0.
5. SLOT_WIDTH = 00 (32 BCLKs), 01 (24 BCLKs), 10 (16 BCLKs).

10296-027

Figure 27. TDM Nonpulse Mode Audio Format



NOTES
1. SAI = 001 (2 CHANNELS), 010 (4 CHANNELS), 011 (8 CHANNELS), 100 (16 CHANNELS)
2. SDATA_FMT = 00 (I²S), 01 (LJ), 10 (RJ, 24-BIT), 11 (RJ, 16-BIT)
3. BCLK_EDGE = 0
4. LRCLK_MODE = 1
5. SLOT_WIDTH = 00 (32 BCLKs), 01 (24 BCLKs), 10 (16 BCLKs)

10296-028

Figure 28. TDM Pulse Mode Audio Format

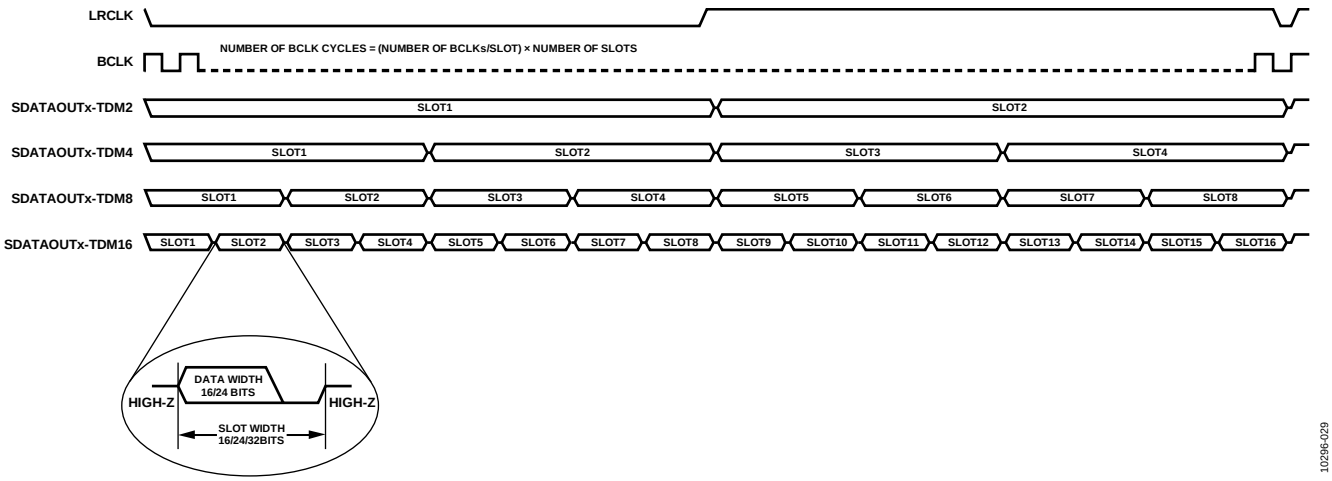


Figure 29. TDM Mode Slot Assignment

The bit clock frequency depends on the sample rate, the slot width, and the number of bit clocks per slot. Table 19 can be used to calculate the BCLK frequency.

The sample rate (f_S) can range from 8 kHz up to 192 kHz. However, in master mode, the maximum bit clock frequency (BCLK) is 24.576 MHz. For example, for a sample rate of 192 kHz, 128 × f_S is the maximum possible BCLK frequency. Therefore, only 128 bit clock cycles are available per TDM frame. There are two options in this case: either operate with a 32-bit data width in TDM4 or operate with a 16-bit data width in TDM8. In slave mode, this limitation does not exist because the bit clock and frame clock are fed to the ADAU1977. Various combinations of BCLK frequency and mode are available, but care must be taken to choose the combination that is most suitable for the application.

Connection Options

Figure 30 through Figure 34 show the available options for connecting the serial audio port in I²S or TDM mode. In TDM mode, it is recommended to include the pull-down resistor on the data signal to prevent the line from floating when the SDATAOUTx pin of ADAU1977 goes high-Z during an inactive period. The resistor value should be such that no more than 2 mA is drawn from the SDATAOUTx pin. Although the resistor value is typically in the range of 10 kΩ to 47 kΩ, the appropriate resistor value depends on the devices on the data bus.

Table 19. Bit Clock Frequency TDM Mode

	BCLK Frequency		
Mode	**16 Bit Clocks Per Slot**	**24 Bit Clocks Per Slot**	**32 Bit Clocks Per Slot**
TDM2	32 × f_S	48 × f_S	64 × f_S
TDM4	64 × f_S	96 × f_S	128 × f_S
TDM8	128 × f_S	192 × f_S	256 × f_S
TDM16	256 × f_S	384 × f_S	512 × f_S

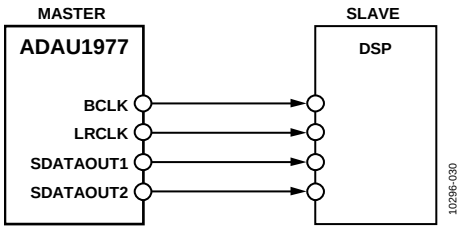


Figure 30. Serial Port Connection Option 1—I²S/LJ/RJ Mode, ADAU1977 Master

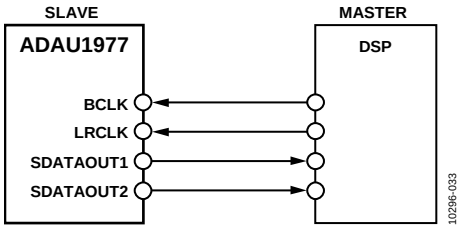


Figure 31. Serial Port Connection Option 2—I²S/LJ/RJ Mode, ADAU1977 Slave

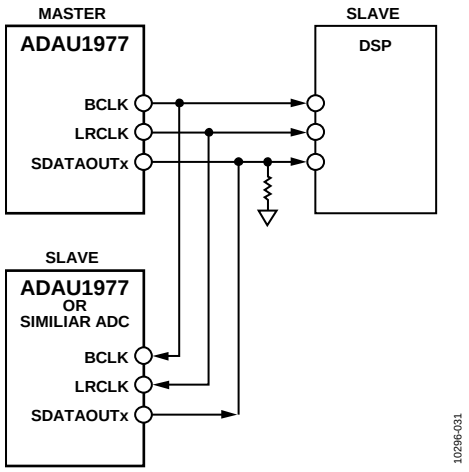


Figure 32. Serial Port Connection Option 3—TDM Mode, ADAU1977 Master

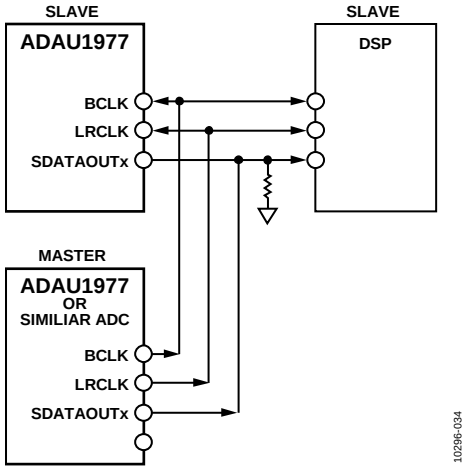


Figure 33. Serial Port Connection Option 4—TDM Mode, Second ADC Master

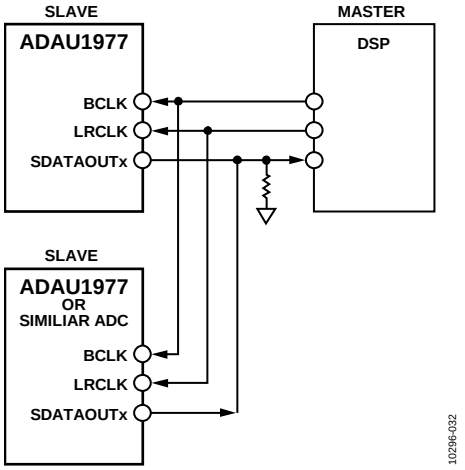


Figure 34. Serial Port Connection Option 5—TDM Mode, DSP Master

CONTROL PORTS

The ADAU1977 control port allows two modes of operation—either 2-wire I²C mode or 4-wire SPI mode—that are used for setting the internal registers of the part. Both the I²C and SPI modes allow read and write capability of the registers. All the registers are eight bits wide. The registers start at Address 0x00 and end at Address 0x1A.

The control port in both I²C and SPI modes is slave only and, therefore, requires the master in the system to operate. The registers can be accessed with or without the master clock to the part. However, to operate the PLL, serial audio ports, and boost converter, the master clock is necessary.

By default, the ADAU1977 operates in I²C mode, but the part can be put into SPI mode by pulling the $\overline{\text{CLATCH}}$ pin low three times.

The control port pins are multifunctional, depending on the mode in which the part is operating. Table 20 describes the control port pin functions in both modes.

Table 20. Control Port Pin Functions

		I²C Mode		SPI Mode	
Pin No.	**Pin Name**	**Pin Functions**	**Pin Type**	**Pin Functions**	**Pin Type**
17	SDA/COUT	SDA: data	I/O	COUT: output data	O
18	SCL/CCLK	SCL: clock	I	$\overline{\text{CCLK}}$: input clock	I
19	ADDR0/$\overline{\text{CLATCH}}$	I²C Device Address Bit 0	I	$\overline{\text{CLATCH}}$: input	I
20	ADDR1/CIN	I²C Device Address Bit 1	I	CIN: input data	I

I²C MODE

The ADAU1977 supports a 2-wire serial (I²C-compatible) bus protocol. Two pins—serial data (SDA) and serial clock (SCL)—are used to communicate with the system I²C master controller. In I²C mode, the ADAU1977 is always a slave on the bus, meaning that it cannot initiate a data transfer. Each slave device on the I²C bus is recognized by a unique device address. The device address and R/$\overline{W}$ byte for the ADAU1977 are shown in Table 21. The address resides in the first seven bits of the I²C write. Bit 7 and Bit 6 of the I²C address for the ADAU1977 are set by the levels on the ADDR1 and ADDR0 pins. The LSB of the first I²C byte (the R/$\overline{W}$ bit) from the master identifies whether it is a read or write operation. Logic Level 1 in LSB corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Table 21. ADAU1977 I²C First Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR1	ADDR0	1	0	0	0	1	R/$\overline{W}$

The first seven bits of the I²C chip address for the ADAU1977 are xx10001. Bit 0 and Bit 1 of the address byte can be set using the ADDR1 and ADDR0 pins to set the chip address to the desired value.

The 7-bit I²C device address can be set to one of four possible options using the ADDR1 and ADDR0 pins:

- I²C Device Address 0010001 (0x11)
- I²C Device Address 0110001 (0x31)
- I²C Device Address 1010001 (0x51)
- I²C Device Address 1110001 (0x71)

In I²C mode, both the SDA and SCL pins require that an appropriate pull-up resistor be connected to IOVDD. The voltage on these signal lines should not exceed the voltage on the IOVDD pin. Figure 46 shows a typical connection diagram for the I²C mode.

The value of the pull-up resistor for the SDA or SCL pin can be calculated as follows.

$$Minimum\ R_{PULL\ UP} = (IOVDD - V_{IL})/I_{SINK}$$

where:
IOVDD is the I/O supply voltage, typically ranging from 1.8 V up to 3.3 V.
V_{IL} is the maximum voltage at Logic Level 0 (that is, 0.4 V, as per the I²C specifications).
I_{SINK} is the current sink capability of the I/O pin.

The SDA pin can sink 2 mA current; therefore, the minimum value of $R_{PULL\ UP}$ for an IOVDD of 3.3 V is 1.5 kΩ.

Depending on the capacitance of the board, the speed of the bus can be restricted to meet the rise time and fall time specifications.

For fast mode with a bit rate time of around 1 Mbps, the rise time must be less than 550 ns. Use the following equation to determine whether the rise time specification can be met:

$$t = 0.8473 \times R_{PULL\ UP} \times C_{BOARD}.$$

To meet the 300 ns rise time requirement, the C_{BOARD} must be less than 236 pF.

For the SCL pin, the calculations depend on the current sink capability of the I²C master used in the system.

Addressing

Initially, each device on the I²C bus is in an idle state and monitors the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and acquire the next eight bits from the master (the 7-bit address plus the R/$\overline{W}$ bit) MSB first. The master sends the 7-bit device address with the read/write bit to all the slaves on the bus. The device with the matching address responds by pulling the data line (SDA) low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition.

The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master is to write information to the slave, whereas a Logic 1 means that the master is to read information from the slave after writing the address and repeating the start address. A data transfer takes place until a master initiates a stop condition. A stop condition occurs when SDA transitions from low to high while SCL is held high.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence during normal read and write operations, the ADAU1977 immediately jumps to the idle condition.

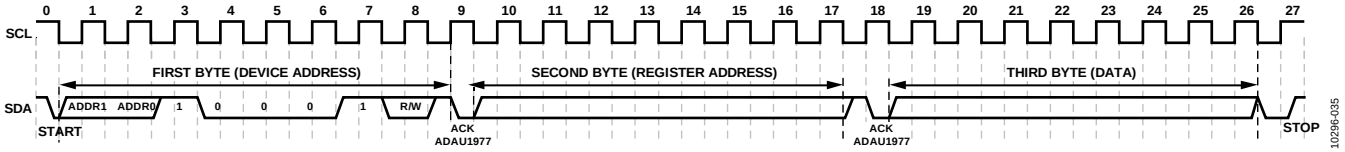


Figure 35. I²C Write to ADAU1977 Single Byte

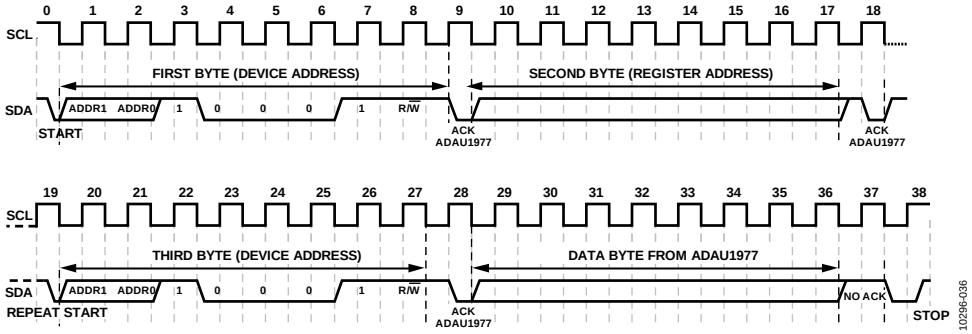


Figure 36. I²C Read from ADAU1977 Single Byte

I²C Read and Write Operations

Figure 37 shows the format of a single-word write operation. Every ninth clock pulse, the ADAU1977 issues an acknowledge by pulling SDA low.

Figure 38 shows the format of a burst mode write sequence. This figure shows an example of a write to sequential single-byte registers. The ADAU1977 increments its address register after every byte because the requested address corresponds to a register or memory area with a 1-byte word length.

Figure 39 shows the format of a single-word read operation. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation. This is because the address still needs to be written to set up the internal address. After the ADAU1977 acknowledges the receipt of the address, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ bit set to 1 (read). This causes the ADAU1977 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1977.

Figure 40 shows the format of a burst mode read sequence. This figure shows an example of a read from sequential single-byte registers. The ADAU1977 increments its address registers after every byte because the ADAU1977 uses an 8-bit register address.

Figure 37 to Figure 40 use the following abbreviations:
S = start bit
P = stop bit
AM = acknowledge by master
AS = acknowledge by slave

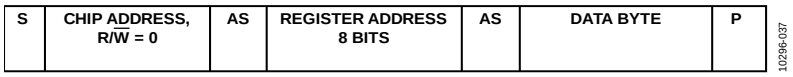


Figure 37. Single-Word I²C Write Format

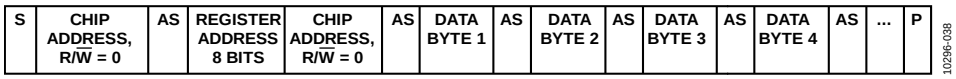


Figure 38. Burst Mode I²C Write Format

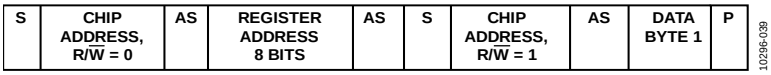


Figure 39. Single-Word I²C Read Format

Figure 40. Burst Mode I²C Read Format

SPI MODE

By default, the ADAU1977 is in I²C mode. To invoke SPI control mode, pull $\overline{\text{CLATCH}}$ low three times. This can be done by performing three dummy writes to the SPI port (the ADAU1977 does not acknowledge these three writes; see Figure 41). Beginning with the fourth SPI write, data can be written to or read from the device. The ADAU1977 can be taken out of SPI mode only by a full reset initiated by power cycling the device.

The SPI port uses a 4-wire interface, consisting of the $\overline{\text{CLATCH}}$, CCLK, CIN, and COUT signals, and it is always a slave port. The $\overline{\text{CLATCH}}$ signal should go low at the beginning of a transaction and high at the end of a transaction. The CCLK signal latches CDATA on a low-to-high transition. COUT data is shifted out of the ADAU1977 on the falling edge of CCLK and should be clocked into a receiving device, such as a microcontroller, on the CCLK rising edge. The CDATA signal carries the serial input data, and the COUT signal carries the serial output data. The COUT signal remains tristated until a read operation is requested. This allows direct connection to other SPI-compatible peripheral COUT ports for sharing the same system controller port. All SPI transactions have the same basic format shown in Table 24. A timing diagram is shown in Figure 3. All data should be written MSB first.

Chip Address R/$\overline{W}$

The LSB of the first byte of an SPI transaction is a R/$\overline{W}$ bit. This bit determines whether the communication is a read (Logic Level 1) or a write (Logic Level 0). This format is shown in Table 22.

Table 22. ADAU1977 SPI Address and R/$\overline{W}$ Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	R/$\overline{W}$

Register Address

The 8-bit address word is decoded to a location in one of the registers. This address is the location of the appropriate register.

Data Bytes

The number of data bytes varies according to the register being accessed. During a burst mode write, an initial register address is written followed by a continuous sequence of data for consecutive register locations.

A sample timing diagram for a single-word SPI write operation to a register is shown in Figure 42. A sample timing diagram of a single-word SPI read operation is shown in Figure 43. The COUT pin goes from being high-Z to being driven at the beginning of Byte 3. In this example, Byte 0 to Byte 1 contain the device address, the R/$\overline{W}$ bit, and the register address to be read. Subsequent bytes carry the data from the device.

Standalone Mode

The ADAU1977 can also be operated in standalone mode. However, in standalone mode, the boost converter, microphone bias, and diagnostics blocks are powered down. To set the part in standalone mode, pull the SA_MODE pin to IOVDD. In this mode, some pins change functionality to provide more flexibility (see Table 23 for more information).

Table 23. Pin Functionality in Standalone Mode

Pin Function	Setting	Description
ADDR0	0	I²S SAI format
	1	TDM modes, determined by the SDATAOUT2 pin
ADDR1	0	Master mode SAI
	1	Slave mode SAI
SDA	0	MCLK = 256 × f_S, PLL on
	1	MCLK = 384 × f_S, PLL on
SCL	0	48 kHz sample rate
	1	96 kHz sample rate
SDATAOUT2	0	TDM4—LRCLK pulse
	1	TDM8—LRCLK pulse
FAULT	0	Slot 1 to Slot 4 in TDM8
	1	Slot 5 to Slot 8 in TDM8

If set for TDM8 mode, the FAULT pin is used as an input for assigning the ADC data slot to prevent collision with other data on TDM bus.

Table 24. Generic Control Word Format

Byte 0	Byte 1	Byte 2	Byte 3[1]
Device Address[6:0], R/$\overline{W}$	Register Address[7:0]	Data[7:0]	Data[7:0]

[1] Continues to end of data.

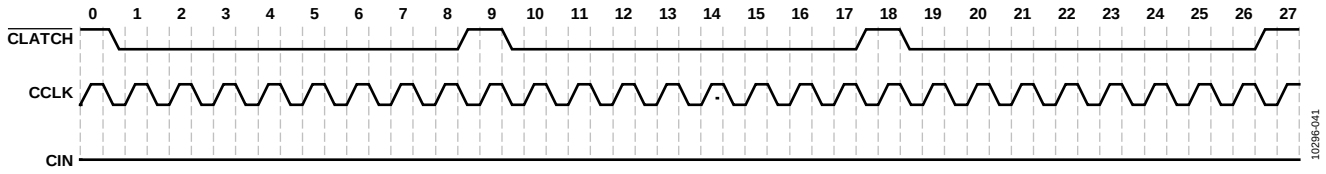


Figure 41. SPI Mode Initial Sequence

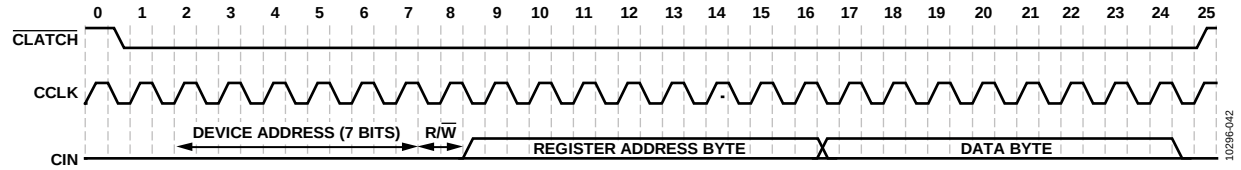


Figure 42. SPI Write to ADAU1977 Clocking (Single-Word Write Mode)

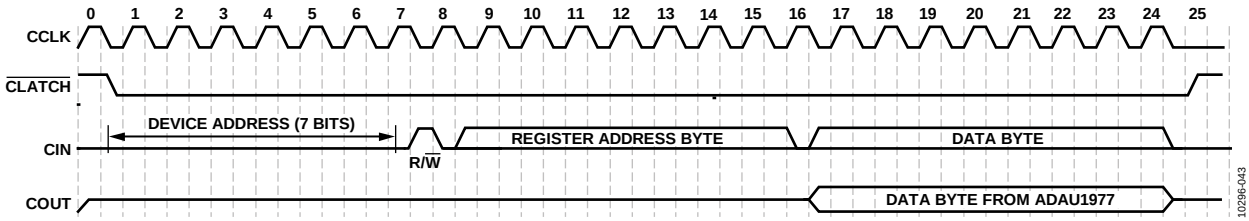


Figure 43. SPI Read from ADAU1977 Clocking (Single-Word Read Mode)

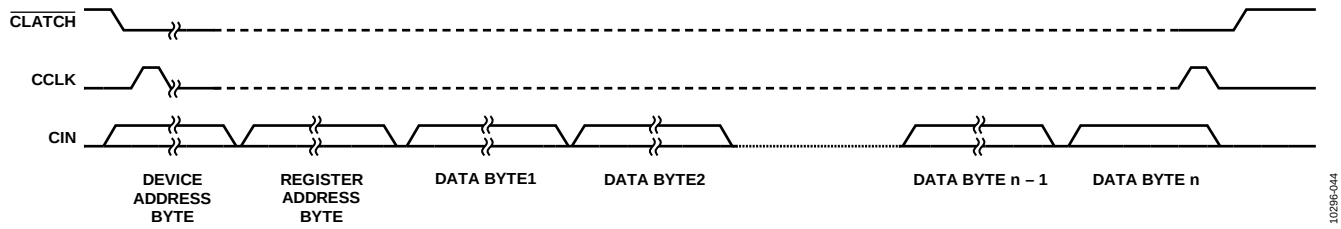


Figure 44. SPI Write to ADAU1977 (Multiple Bytes)

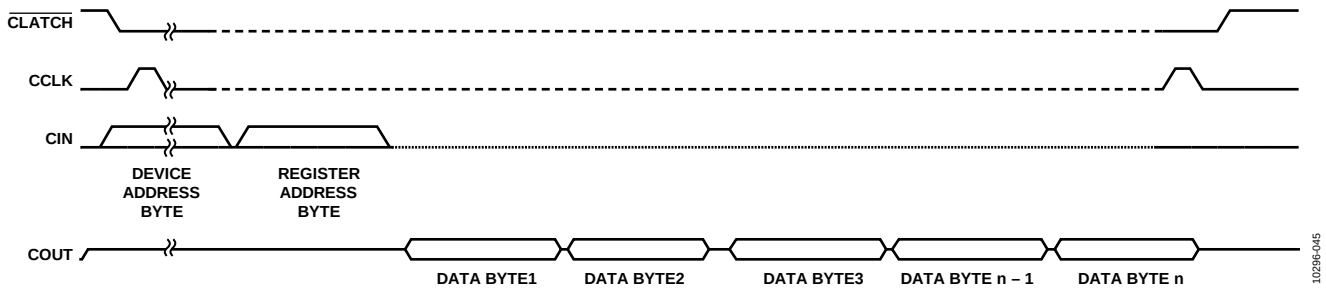


Figure 45. SPI Read from ADAU1977 (Multiple Bytes)

REGISTER SUMMARY

Table 25 is the control register summary. The registers can be accessed using the I²C control port or the SPI control port.

Table 25. ADAU1977 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	M_POWER	[7:0]	S_RST	RESERVED						PWUP	0x00	RW
0x01	PLL_CONTROL	[7:0]	PLL_LOCK	PLL_MUTE	RESERVED	CLK_S	RESERVED	MCS			0x41	RW
0x02	BST_CONTROL	[7:0]	BST_GOOD	FS_RATE		BOOST_SW_FREQ	OV_EN	BOOST_OV	OC_EN	BOOST_OC	0x4A	RW
0x03	MB_BST_CONTROL	[7:0]	MB_VOLTS				MB_EN	BOOST_EN	MRCV	BOOST_RCVR	0x7D	RW
0x04	BLOCK_POWER_SAI	[7:0]	LR_POL	BCLKEDGE	LDO_EN	VREF_EN	ADC_EN4	ADC_EN3	ADC_EN2	ADC_EN1	0x3F	RW
0x05	SAI_CTRL0	[7:0]	SDATA_FMT		SAI			FS			0x02	RW
0x06	SAI_CTRL1	[7:0]	SDATA_SEL	SLOT_WIDTH		DATA_WIDTH	LR_MODE	SAI_MSB	BCLKRATE	SAI_MS	0x00	RW
0x07	SAI_CMAP12	[7:0]	CMAP_C2				CMAP_C1				0x10	RW
0x08	SAI_CMAP34	[7:0]	CMAP_C4				CMAP_C3				0x32	RW
0x09	SAI_OVERTEMP	[7:0]	SAI_DRV_C4	SAI_DRV_C3	SAI_DRV_C2	SAI_DRV_C1	DRV_HIZ	OT_MCRV	OT_RCVR	OT	0xF0	RW
0x0A	POSTADC_GAIN1	[7:0]	PADC_GAIN1								0xA0	RW
0x0B	POSTADC_GAIN2	[7:0]	PADC_GAIN2								0xA0	RW
0x0C	POSTADC_GAIN3	[7:0]	PADC_GAIN3								0xA0	RW
0x0D	POSTADC_GAIN4	[7:0]	PADC_GAIN4								0xA0	RW
0x0E	MISC_CONTROL	[7:0]	SUM_MODE		RESERVED	MMUTE	RESERVED			DC_CAL	0x02	RW
0x10	DIAG_CONTROL	[7:0]	RESERVED				DIAG_EN4	DIAG_EN3	DIAG_EN2	DIAG_EN1	0x0F	RW
0x11	DIAG_STATUS1	[7:0]	RESERVED	MIC_SHORT1	MICH_OPEN1	MICH_SB1	MICH_SG1	MICH_SMB1	MICL_SB1	MICL_SG1	0x00	RW
0x12	DIAG_STATUS2	[7:0]	RESERVED	MIC_SHORT2	MIC_OPEN2	MICH_SB2	MICH_SG2	MICH_SMB2	MICL_SB2	MICL_SG2	0x00	RW
0x13	DIAG_STATUS3	[7:0]	RESERVED	MIC_SHORT3	MIC_OPEN3	MICH_SB3	MICH_SG3	MICH_SMB3	MICL_SB3	MICL_SG3	0x00	RW
0x14	DIAG_STATUS4	[7:0]	RESERVED	MIC_SHORT4	MIC_OPEN4	MICH_SB4	MICH_SG4	MICH_SMB4	MICL_SB4	MICL_SG4	0x00	RW
0x15	DIAG_IRQ1	[7:0]	RESERVED	IRQ_RESET	IRQ_DRIVE	IRQ_POL	DIAG_MASK4	DIAG_MASK3	DIAG_MASK2	DIAG_MASK1	0x20	RW
0x16	DIAG_IRQ2	[7:0]	BST_FAULT_MASK	MIC_SHORT_MASK	MIC_OPEN_MASK	MICH_SB_MASK	MICH_SG_MASK	RESERVED	MICL_SB_MASK	MICL_SG_MASK	0x00	RW
0x17	DIAG_ADJUST1	[7:0]	SHT_T_TRIP		SHT_M_TRIP		SHT_G_TRIP		SHT_B_TRIP		0x00	RW
0x18	DIAG_ADJUST2	[7:0]	RESERVED		FAULT_TO		RESERVED	HYST_SM_EN	HYST_SG_EN	HYST_SB_EN	0x20	RW
0x19	ASDC_CLIP	[7:0]	RESERVED				ADC_CLIP4	ADC_CLIP3	ADC_CLIP2	ADC_CLIP1	0x00	RW
0x1A	DC_HPF_CAL	[7:0]	DC_SUB_C4	DC_SUB_C3	DC_SUB_C2	DC_SUB_C1	DC_HPF_C4	DC_HPF_C3	DC_HPF_C2	DC_HPF_C1	0x00	RW

REGISTER DETAILS

MASTER POWER AND SOFT RESET REGISTER

Address: 0x00, Reset: 0x00, Name: M_POWER

The power management control register is used for enabling boost regulator, microphone bias, PLL, band gap reference, ADC, and LDO regulator.

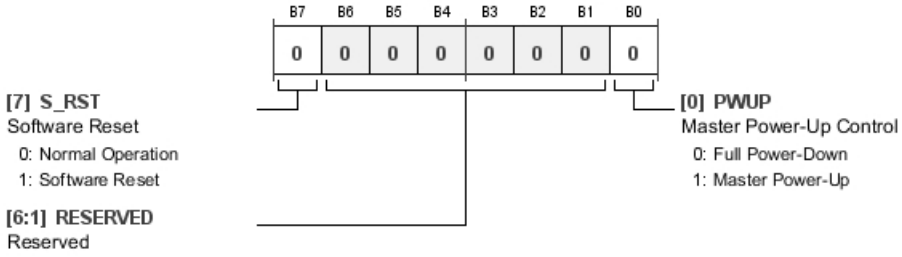


Table 26. Bit Descriptions for M_POWER

Bits	Bit Name	Settings	Description	Reset	Access
7	S_RST		Software Reset. The software reset resets all internal circuitry and places all control registers to their default state. It is not necessary to reset the ADAU1977 during a power-up or power-down cycle.	0x0	RW
		0	Normal Operation		
		1	Software Reset		
[6:1]	RESERVED		Reserved.	0x00	RW
0	PWUP		Master Power-Up Control. The master power-up control fully powers up or powers down the ADAU1977. This must be set to 1 to power up the ADAU1977. Individual blocks can be powered down via their respective power control registers.	0x0	RW
		0	Full Power-Down		
		1	Master Power-Up		

PLL CONTROL REGISTER

Address: 0x01, Reset: 0x41, Name: PLL_CONTROL

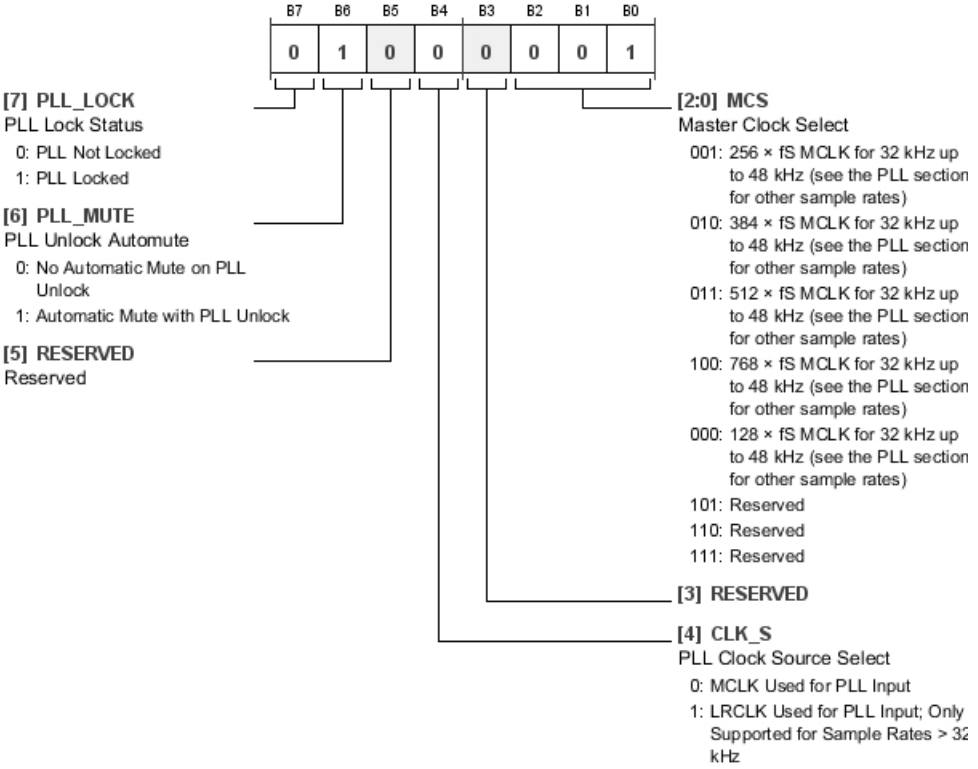


Table 27. Bit Descriptions for PLL_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
7	PLL_LOCK		PLL Lock Status. PLL lock status bit. When one PLL is locked.	0x0	R
		0	PLL Not Locked		
		1	PLL Locked		
6	PLL_MUTE		PLL Unlock Automute. When set to 1, mutes the ADC output if PLL becomes unlocked.	0x1	RW
		0	No Automatic Mute on PLL Unlock		
		1	Automatic Mute with PLL Unlock		
5	RESERVED		Reserved.	0x0	RW
4	CLK_S		PLL Clock Source Select. Selecting input clock source for PLL.	0x0	RW
		0	MCLK Used for PLL Input		
		1	LRCLK Used for PLL Input; Only Supported for Sample Rates > 32 kHz		
[2:0]	MCS		Master Clock Select. MCS bits determine the frequency multiplication ratio of the PLL. It must be set based on the input MCLK frequency and sample rate.	0x1	RW
		001	256 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL section for other sample rates)		
		010	384 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL section for other sample rates)		
		011	512 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL section for other sample rates)		
		100	768 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL section for other sample rates)		
		000	128 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL section for other sample rates)		

Bits	Bit Name	Settings	Description	Reset	Access
		101	Reserved		
		110	Reserved		
		111	Reserved		

DC-TO-DC BOOST CONVERTER CONTROL REGISTER

Address: 0x02, Reset: 0x4A, Name: BST_CONTROL

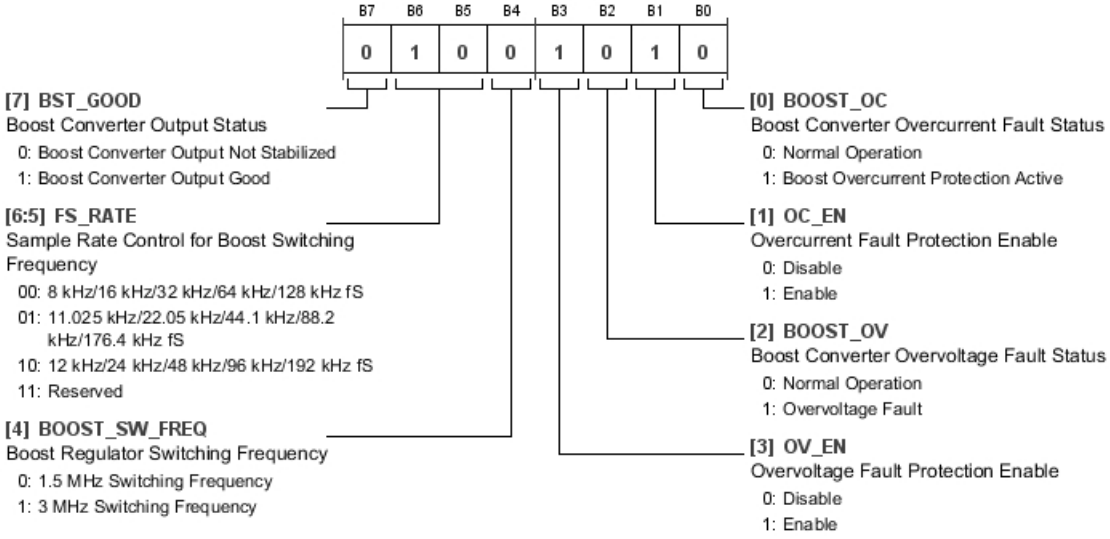


Table 28. Bit Descriptions for BST_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
7	BST_GOOD		Boost Converter Output Status.	0x0	R
		0	Boost Converter Output Not Stabilized		
		1	Boost Converter Output Good		
[6:5]	FS_RATE		Sample Rate Control for Boost Switching Frequency.	0x2	RW
		00	8 kHz/16 kHz/32 kHz/64 kHz/128 kHz f_S		
		01	11.025 kHz/22.05 kHz/44.1 kHz/88.2 kHz/176.4 kHz f_S		
		10	12 kHz/24 kHz/48 kHz/96 kHz/192 kHz f_S		
		11	Reserved		
4	BOOST_SW_FREQ		Boost Regulator Switching Frequency.	0x0	RW
		0	1.5 MHz Switching Frequency		
		1	3 MHz Switching Frequency		
3	OV_EN		Overvoltage Fault Protection Enable.	0x1	RW
		0	Disable		
		1	Enable		
2	BOOST_OV		Boost Converter Overvoltage Fault Status.	0x0	R
		0	Normal Operation		
		1	Overvoltage Fault		
1	OC_EN		Overcurrent Fault Protection Enable.	0x1	RW
		0	Disable		
		1	Enable		
0	BOOST_OC		Boost Converter Overcurrent Fault Status.	0x0	R
		0	Normal Operation		
		1	Boost Overcurrent Protection Active		

MICBIAS AND BOOST CONTROL REGISTER

Address: 0x03, Reset: 0x7D, Name: MB_BST_CONTROL

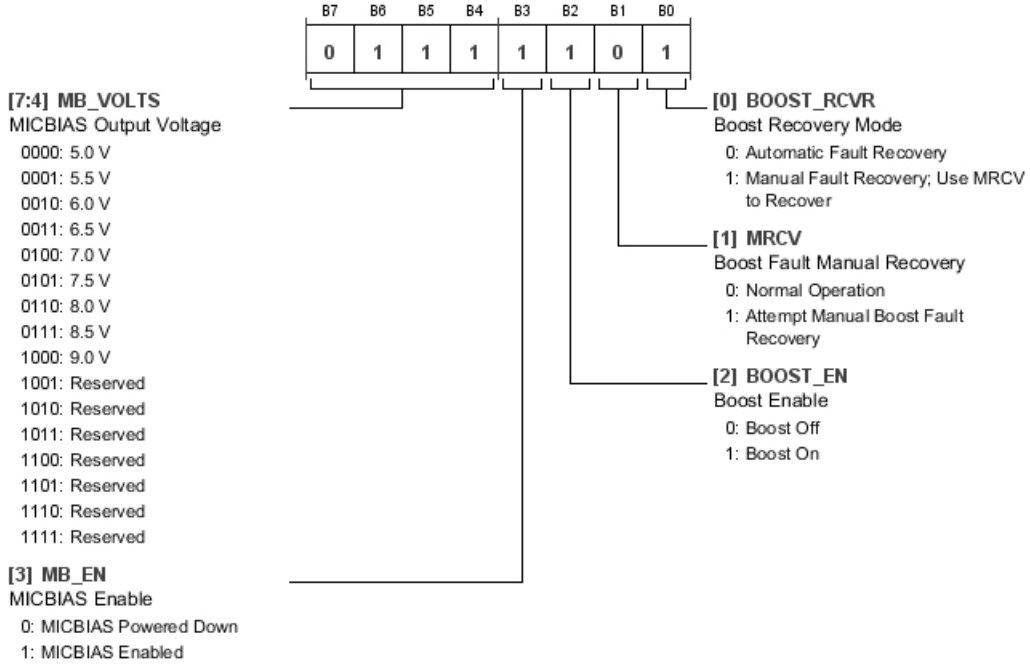


Table 29. Bit Descriptions for MB_BST_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	MB_VOLTS		MICBIAS Output Voltage.	0x7	RW
		0000	5.0 V		
		0001	5.5 V		
		0010	6.0 V		
		0011	6.5 V		
		0100	7.0 V		
		0101	7.5 V		
		0110	8.0 V		
		0111	8.5 V		
		1000	9.0 V		
		1001	Reserved		
		1010	Reserved		
		1011	Reserved		
		1100	Reserved		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		
3	MB_EN		MICBIAS Enable.	0x1	RW
		0	MICBIAS Powered Down		
		1	MICBIAS Enabled		
2	BOOST_EN		Boost Enable.	0x1	RW
		0	Boost Off		
		1	Boost On		
1	MRCV		Boost Fault Manual Recovery.	0x0	W
		0	Normal Operation		
		1	Attempt Manual Boost Fault Recovery		

Bits	Bit Name	Settings	Description	Reset	Access
0	BOOST_RCVR		Boost Recovery Mode.	0x1	RW
		0	Automatic Fault Recovery		
		1	Manual Fault Recovery; Use MRCV to Recover		

BLOCK POWER CONTROL AND SERIAL PORT CONTROL REGISTER

Address: 0x04, Reset: 0x3F, Name: BLOCK_POWER_SAI

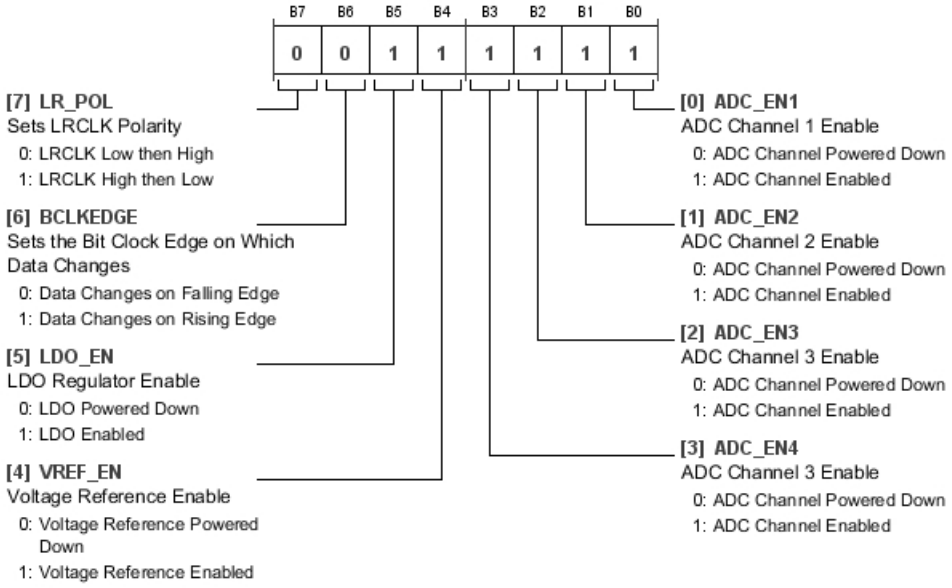


Table 30. Bit Descriptions for BLOCK_POWER_SAI

Bits	Bit Name	Settings	Description	Reset	Access
7	LR_POL		Sets LRCLK Polarity.	0x0	RW
		0	LRCLK Low then High		
		1	LRCLK High then Low		
6	BCLKEDGE		Sets the Bit Clock Edge on Which Data Changes.	0x0	RW
		0	Data Changes on Falling Edge		
		1	Data Changes on Rising Edge		
5	LDO_EN		LDO Regulator Enable.	0x1	RW
		0	LDO Powered Down		
		1	LDO Enabled		
4	VREF_EN		Voltage Reference Enable.	0x1	RW
		0	Voltage Reference Powered Down		
		1	Voltage Reference Enabled		
3	ADC_EN4		ADC Channel 3 Enable.	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		
2	ADC_EN3		ADC Channel 3 Enable.	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		
1	ADC_EN2		ADC Channel 2 Enable.	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		
0	ADC_EN1		ADC Channel 1 Enable.	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		

SERIAL PORT CONTROL REGISTER1

Address: 0x05, Reset: 0x02, Name: SAI_CTRL0

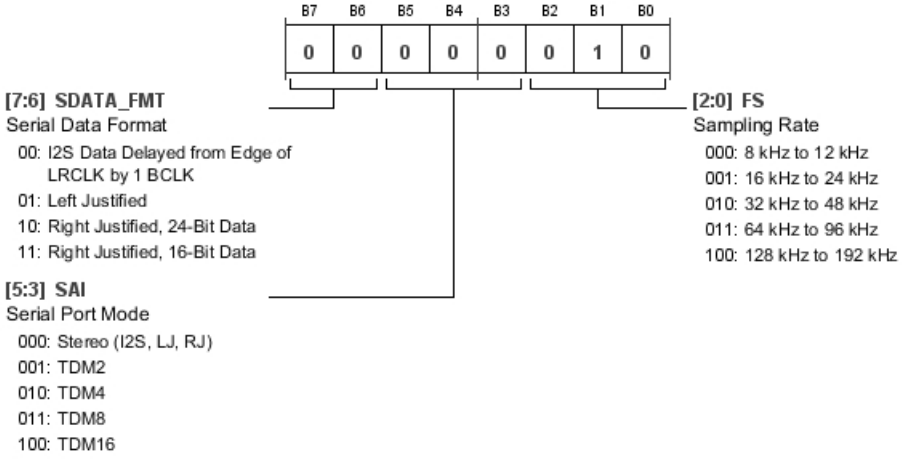


Table 31. Bit Descriptions for SAI_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SDATA_FMT		Serial Data Format.	0x0	RW
		00	I^2S Data Delayed from Edge of LRCLK by 1 BCLK		
		01	Left Justified		
		10	Right Justified, 24-Bit Data		
		11	Right Justified, 16-Bit Data		
[5:3]	SAI		Serial Port Mode.	0x0	RW
		000	Stereo (I^2S, LJ, RJ)		
		001	TDM2		
		010	TDM4		
		011	TDM8		
		100	TDM16		
[2:0]	FS		Sampling Rate.	0x2	RW
		000	8 kHz to 12 kHz		
		001	16 kHz to 24 kHz		
		010	32 kHz to 48 kHz		
		011	64 kHz to 96 kHz		
		100	128 kHz to 192 kHz		

SERIAL PORT CONTROL REGISTER2

Address: 0x06, Reset: 0x00, Name: SAI_CTRL1

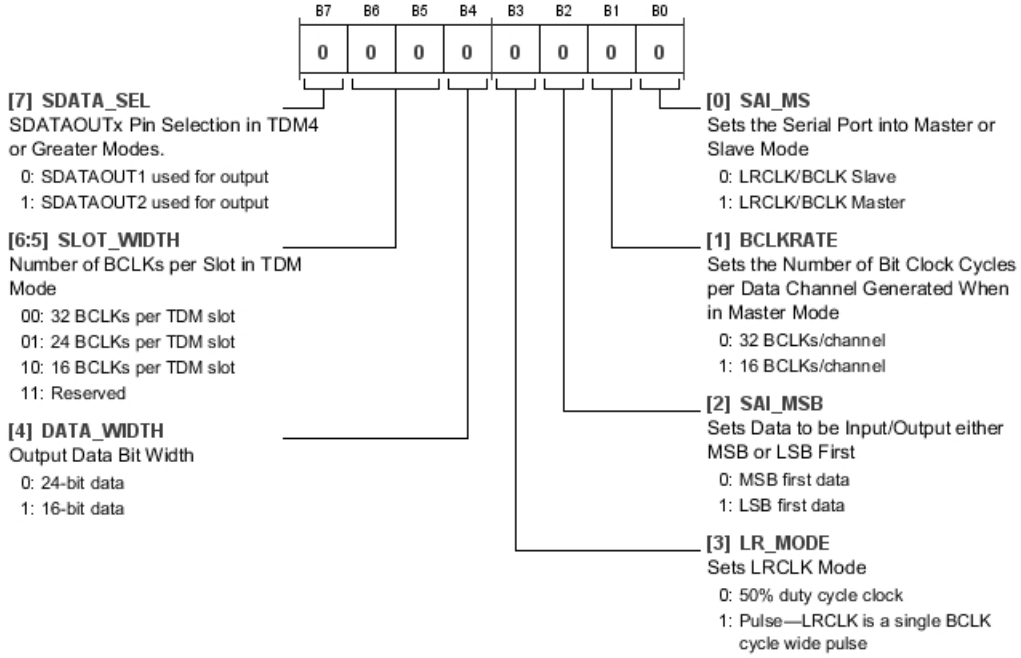


Table 32. Bit Descriptions for SAI_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	SDATA_SEL		SDATAOUTx Pin Selection in TDM4 or Greater Modes.	0x0	RW
		0	SDATAOUT1 used for output		
		1	SDATAOUT2 used for output		
[6:5]	SLOT_WIDTH		Number of BCLKs per Slot in TDM Mode.	0x0	RW
		00	32 BCLKs per TDM slot		
		01	24 BCLKs per TDM slot		
		10	16 BCLKs per TDM slot		
		11	Reserved		
4	DATA_WIDTH		Output Data Bit Width.	0x0	RW
		0	24-bit data		
		1	16-bit data		
3	LR_MODE		Sets LRCLK Mode.	0x0	RW
		0	50% duty cycle clock		
		1	Pulse—LRCLK is a single BCLK cycle wide pulse		
2	SAI_MSB		Sets Data to be Input/Output either MSB or LSB First.	0x0	RW
		0	MSB first data		
		1	LSB first data		
1	BCLKRATE		Sets the Number of Bit Clock Cycles per Data Channel Generated When in Master Mode.	0x0	RW
		0	32 BCLKs/channel		
		1	16 BCLKs/channel		
0	SAI_MS		Sets the Serial Port into Master or Slave Mode.	0x0	RW
		0	LRCLK/BCLK Slave		
		1	LRCLK/BCLK Master		

CHANNEL MAPPING FOR OUTPUT SERIAL PORTS REGISTER

Address: 0x07, Reset: 0x10, Name: SAI_CMAP12

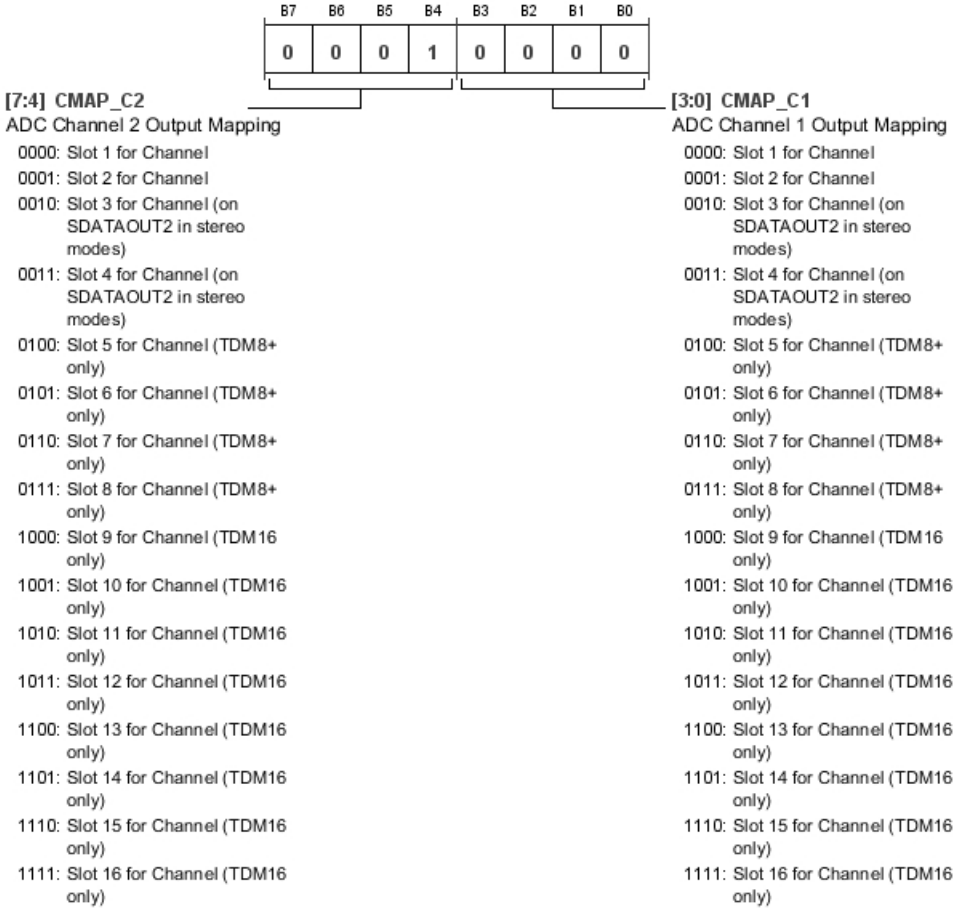


Table 33. Bit Descriptions for SAI_CMAP12

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CMAP_C2		ADC Channel 2 Output Mapping.	0x1	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	CMAP_C1		ADC Channel 1 Output Mapping. If CMAP is set to a slot that doesn't exist for a given serial mode, then that channel will not be driven. For example, if CMAP is set to Slot 9 and the serial format is I2S, then that channel will not be driven. If more than one channel is set to the same slot, only the lowest channel number will be driven; other channels will not be driven.	0x0	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

CHANNEL MAPPING FOR OUTPUT SERIAL PORTS REGISTER

Address: 0x08, Reset: 0x32, Name: SAI_CMAP34

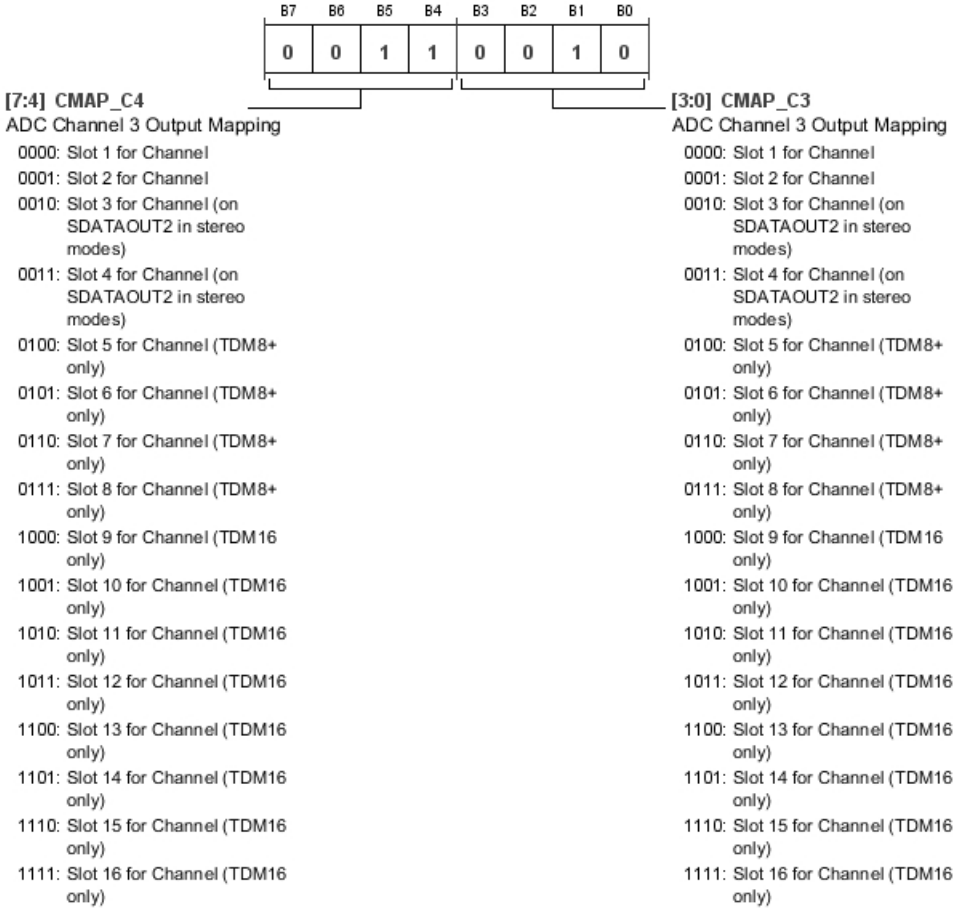


Table 34. Bit Descriptions for SAI_CMAP34

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CMAP_C4		ADC Channel 3 Output Mapping.	0x3	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	CMAP_C3		ADC Channel 3 Output Mapping.	0x2	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

SERIAL OUTPUT DRIVE AND OVERTEMPERATURE PROTECTION CONTROL REGISTER

Address: 0x09, Reset: 0xF0, Name: SAI_OVERTEMP

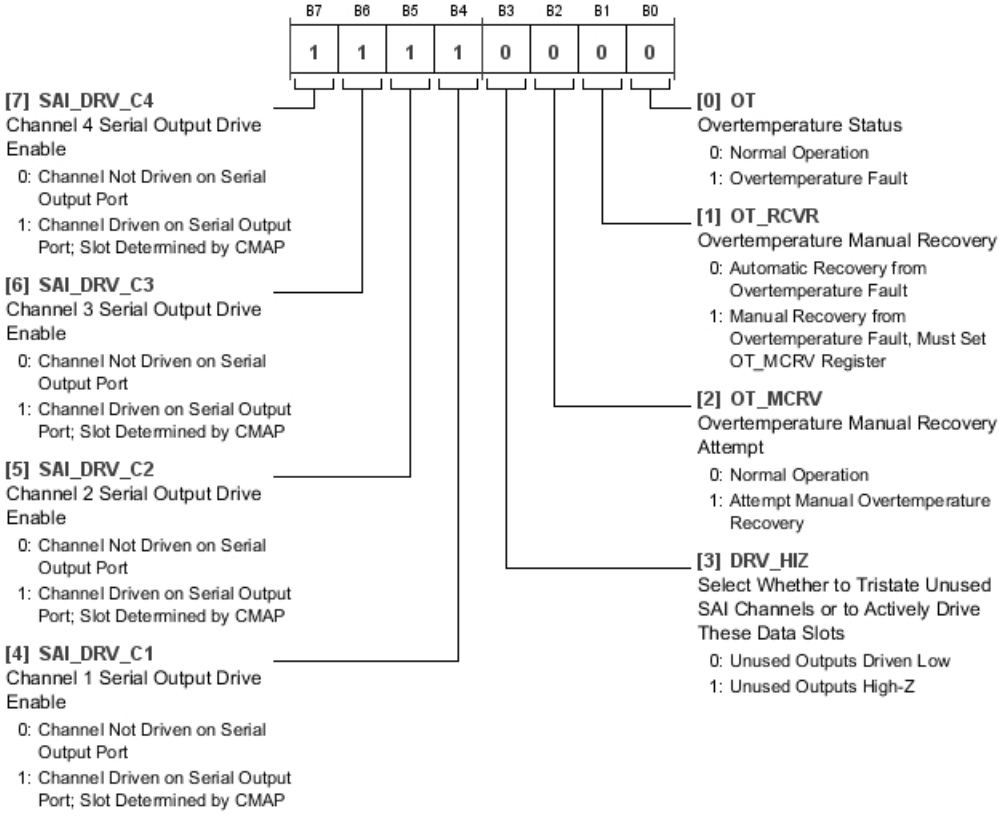


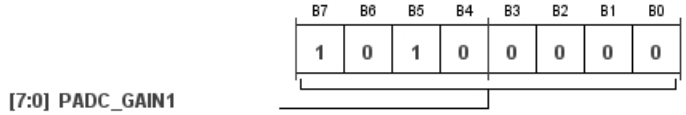
Table 35. Bit Descriptions for SAI_OVERTEMP

Bits	Bit Name	Settings	Description	Reset	Access
7	SAI_DRV_C4		Channel 4 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port		
		1	Channel Driven on Serial Output Port; Slot Determined by CMAP		
6	SAI_DRV_C3		Channel 3 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port		
		1	Channel Driven on Serial Output Port; Slot Determined by CMAP		
5	SAI_DRV_C2		Channel 2 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port		
		1	Channel Driven on Serial Output Port; Slot Determined by CMAP		
4	SAI_DRV_C1		Channel 1 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port		
		1	Channel Driven on Serial Output Port; Slot Determined by CMAP		
3	DRV_HIZ		Select Whether to Tristate Unused SAI Channels or to Actively Drive These Data Slots.	0x0	RW
		0	Unused Outputs Driven Low		
		1	Unused Outputs High-Z		
2	OT_MCRV		Overtemperature Manual Recovery Attempt.	0x0	W
		0	Normal Operation		
		1	Attempt Manual Overtemperature Recovery		
1	OT_RCVR		Overtemperature Manual Recovery.	0x0	RW
		0	Automatic Recovery from Overtemperature Fault		
		1	Manual Recovery from Overtemperature Fault, Must Set OT_MCRV Register		

Bits	Bit Name	Settings	Description	Reset	Access
0	OT		Overtemperature Status.	0x0	R
		0	Normal Operation		
		1	Overtemperature Fault		

POST ADC GAIN CHANNEL 1 CONTROL REGISTER

Address: 0x0A, Reset: 0xA0, Name: POSTADC_GAIN1



[7:0] PADC_GAIN1
Channel 1 Post ADC Gain
00000000: +60 dB Gain
00000001: +59.625 dB Gain
00000010: +59.25 dB Gain
...: ...
10011111: +0.375 dB Gain
10100000: 0 dB Gain
10100001: −0.375 dB Gain
...: ...
11111110: −35.625 dB Gain
11111111: Mute

Table 36. Bit Descriptions for POSTADC_GAIN1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN1		Channel 1 Post ADC Gain.	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

POST ADC GAIN CHANNEL 2 CONTROL REGISTER

Address: 0x0B, Reset: 0xA0, Name: POSTADC_GAIN2

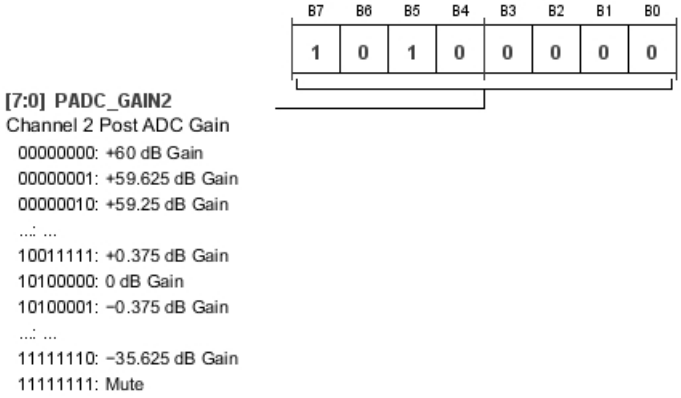
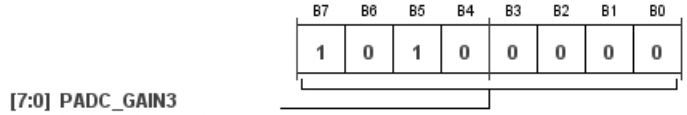


Table 37. Bit Descriptions for POSTADC_GAIN2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN2		Channel 2 Post ADC Gain.	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

POST ADC GAIN CHANNEL 3 CONTROL REGISTER

Address: 0x0C, Reset: 0xA0, Name: POSTADC_GAIN3



[7:0] PADC_GAIN3
Channel 3 Post ADC Gain
00000000: +60 dB Gain
00000001: +59.625 dB Gain
00000010: +59.25 dB Gain
...: ...
10011111: +0.375 dB Gain
10100000: 0 dB Gain
10100001: −0.375 dB Gain
...: ...
11111110: −35.625 dB Gain
11111111: Mute

Table 38. Bit Descriptions for POSTADC_GAIN3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN3		Channel 3 Post ADC Gain.	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

POST ADC GAIN CHANNEL 4 CONTROL REGISTER

Address: 0x0D, Reset: 0xA0, Name: POSTADC_GAIN4

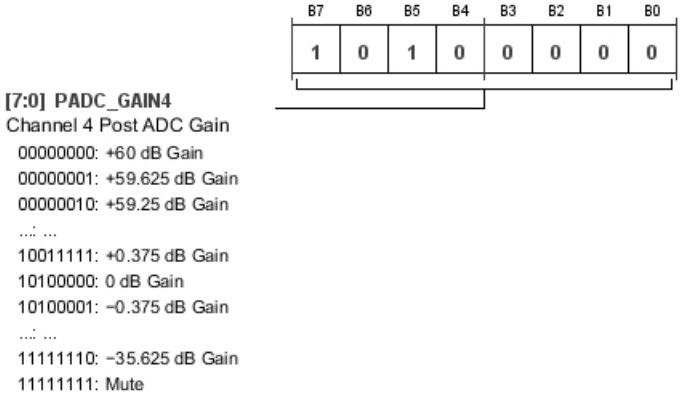


Table 39. Bit Descriptions for POSTADC_GAIN4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN4		Channel 4 Post ADC Gain.	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

HIGH-PASS FILTER AND DC OFFSET CONTROL REGISTER AND MASTER MUTE

Address: 0x0E, Reset: 0x02, Name: MISC_CONTROL

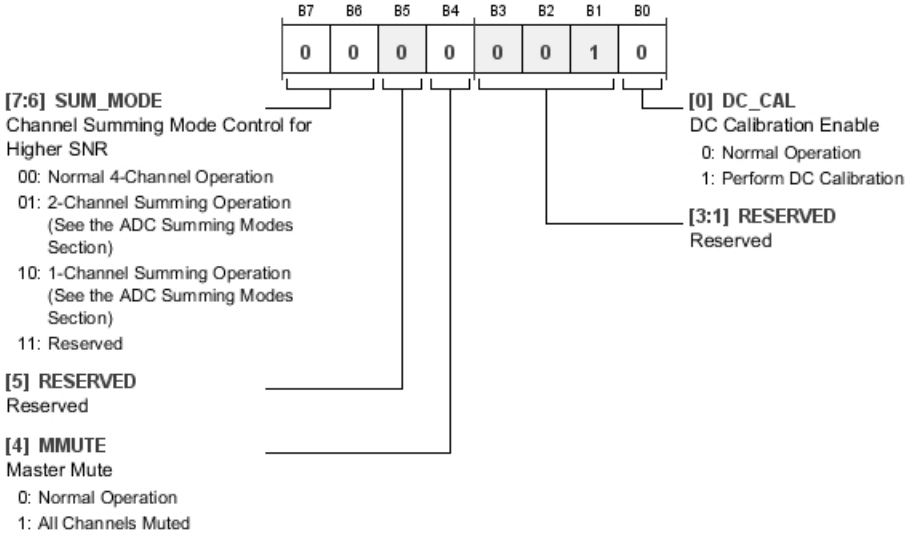


Table 40. Bit Descriptions for MISC_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SUM_MODE		Channel Summing Mode Control for Higher SNR.	0x0	RW
		00	Normal 4-Channel Operation		
		01	2-Channel Summing Operation (See the ADC Summing Modes Section)		
		10	1-Channel Summing Operation (See the ADC Summing Modes Section)		
		11	Reserved		
5	RESERVED		Reserved.	0x0	RW
4	MMUTE		Master Mute.	0x0	RW
		0	Normal Operation		
		1	All Channels Muted		
[3:1]	RESERVED		Reserved.	0x1	RW
0	DC_CAL		DC Calibration Enable.	0x0	RW
		0	Normal Operation		
		1	Perform DC Calibration		

DIAGNOSTICS CONTROL REGISTER

Address: 0x10, Reset: 0x0F, Name: DIAG_CONTROL

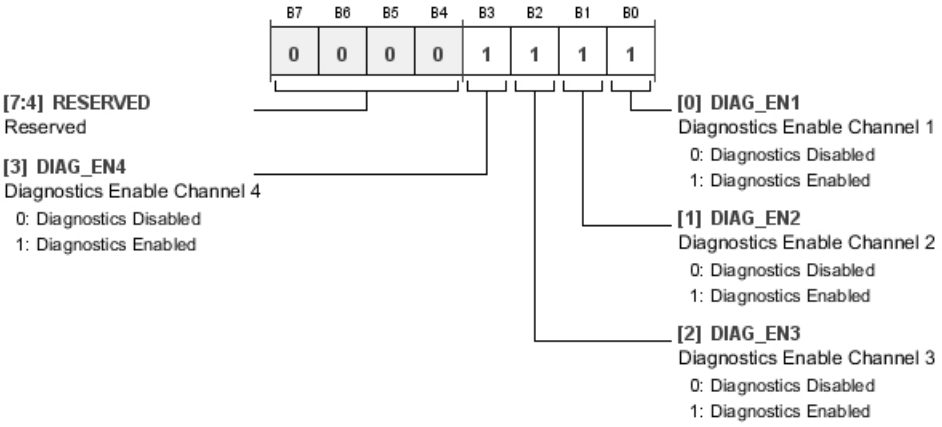


Table 41. Bit Descriptions for DIAG_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
3	DIAG_EN4		Diagnostics Enable Channel 4.	0x1	RW
		0	Diagnostics Disabled		
		1	Diagnostics Enabled		
2	DIAG_EN3		Diagnostics Enable Channel 3.	0x1	RW
		0	Diagnostics Disabled		
		1	Diagnostics Enabled		
1	DIAG_EN2		Diagnostics Enable Channel 2.	0x1	RW
		0	Diagnostics Disabled		
		1	Diagnostics Enabled		
0	DIAG_EN1		Diagnostics Enable Channel 1.	0x1	RW
		0	Diagnostics Disabled		
		1	Diagnostics Enabled		

DIAGNOSTICS REPORT REGISTER CHANNEL 1

Address: 0x11, Reset: 0x00, Name: DIAG_STATUS1

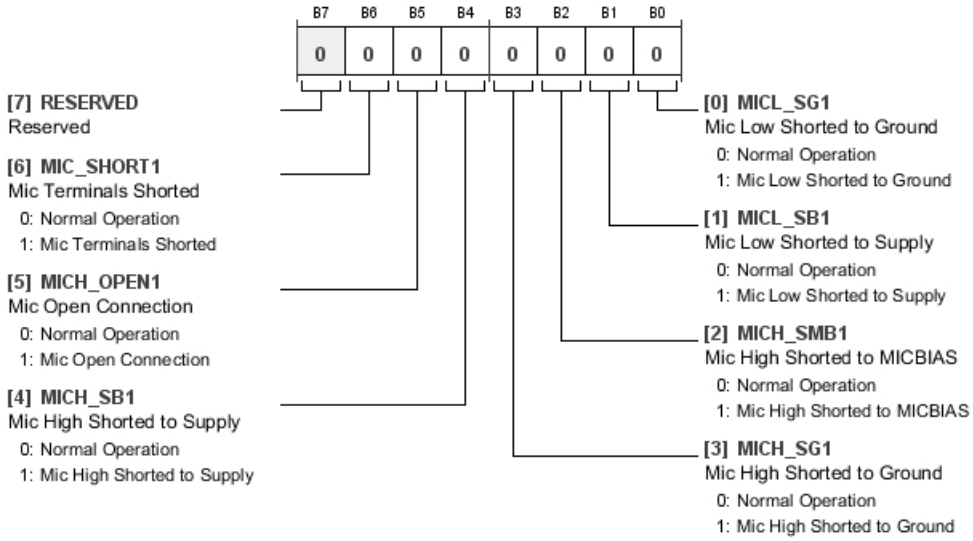


Table 42. Bit Descriptions for DIAG_STATUS1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	MIC_SHORT1		Mic Terminals Shorted.	0x0	R
		0	Normal Operation		
		1	Mic Terminals Shorted		
5	MICH_OPEN1		Mic Open Connection.	0x0	R
		0	Normal Operation		
		1	Mic Open Connection		
4	MICH_SB1		Mic High Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Supply		
3	MICH_SG1		Mic High Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Ground		
2	MICH_SMB1		Mic High Shorted to MICBIAS.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to MICBIAS		
1	MICL_SB1		Mic Low Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Supply		
0	MICL_SG1		Mic Low Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Ground		

DIAGNOSTICS REPORT REGISTER CHANNEL 2

Address: 0x12, Reset: 0x00, Name: DIAG_STATUS2

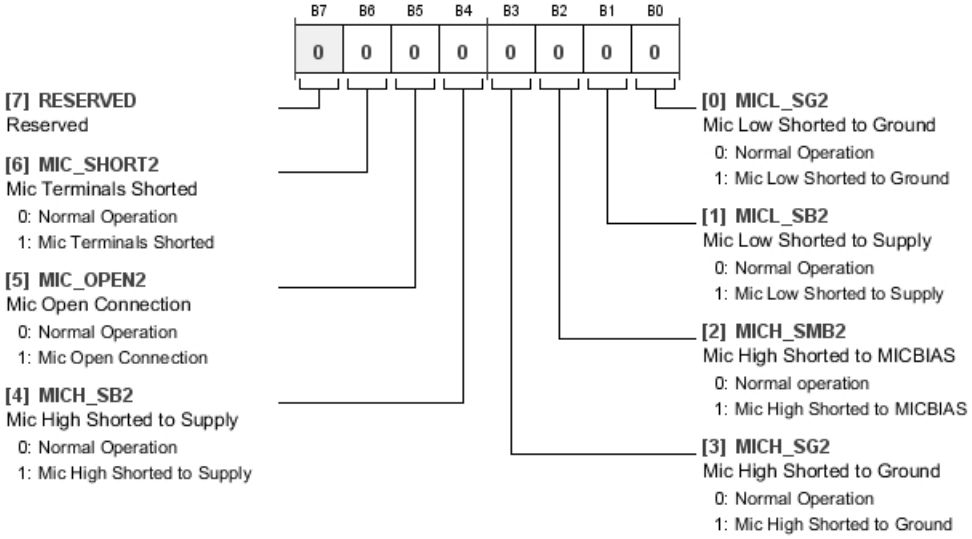


Table 43. Bit Descriptions for DIAG_STATUS2

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	MIC_SHORT2		Mic Terminals Shorted.	0x0	R
		0	Normal Operation		
		1	Mic Terminals Shorted		
5	MIC_OPEN2		Mic Open Connection.	0x0	R
		0	Normal Operation		
		1	Mic Open Connection		
4	MICH_SB2		Mic High Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Supply		
3	MICH_SG2		Mic High Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Ground		
2	MICH_SMB2		Mic High Shorted to MICBIAS.	0x0	R
		0	Normal operation		
		1	Mic High Shorted to MICBIAS		
1	MICL_SB2		Mic Low Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Supply		
0	MICL_SG2		Mic Low Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Ground		

DIAGNOSTICS REPORT REGISTER CHANNEL 3

Address: 0x13, Reset: 0x00, Name: DIAG_STATUS3

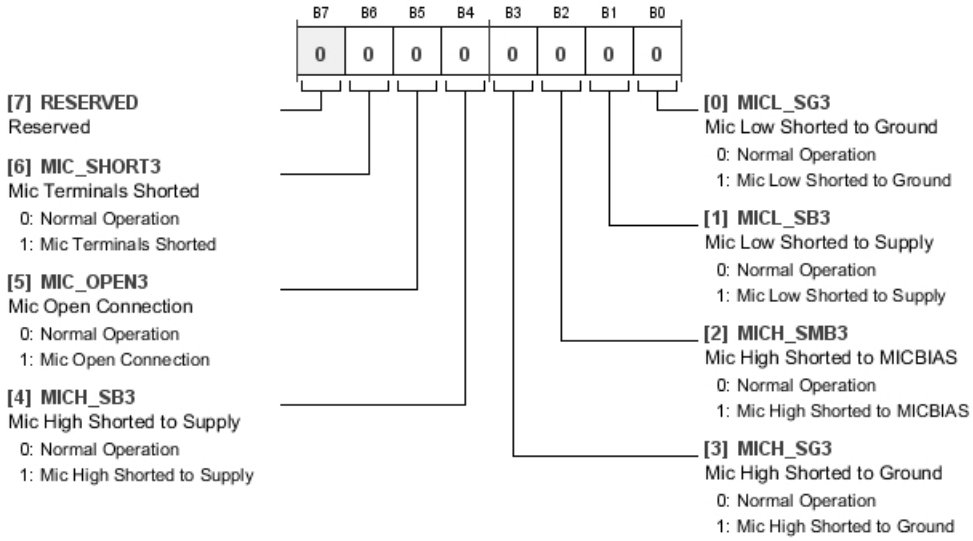


Table 44. Bit Descriptions for DIAG_STATUS3

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	MIC_SHORT3		Mic Terminals Shorted.	0x0	R
		0	Normal Operation		
		1	Mic Terminals Shorted		
5	MIC_OPEN3		Mic Open Connection.	0x0	R
		0	Normal Operation		
		1	Mic Open Connection		
4	MICH_SB3		Mic High Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Supply		
3	MICH_SG3		Mic High Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Ground		
2	MICH_SMB3		Mic High Shorted to MICBIAS.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to MICBIAS		
1	MICL_SB3		Mic Low Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Supply		
0	MICL_SG3		Mic Low Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Ground		

DIAGNOSTICS REPORT REGISTER CHANNEL 4

Address: 0x14, Reset: 0x00, Name: DIAG_STATUS4

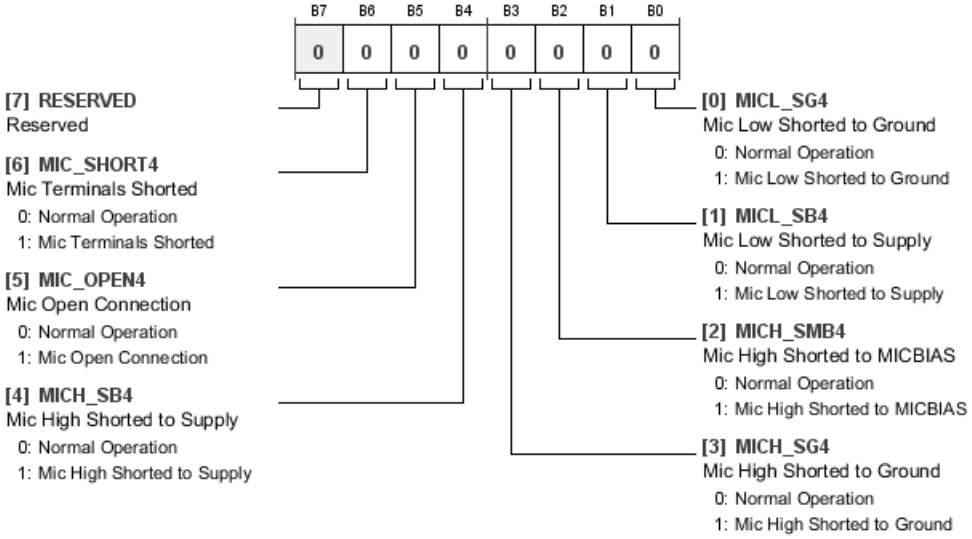


Table 45. Bit Descriptions for DIAG_STATUS4

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	MIC_SHORT4		Mic Terminals Shorted.	0x0	R
		0	Normal Operation		
		1	Mic Terminals Shorted		
5	MIC_OPEN4		Mic Open Connection.	0x0	R
		0	Normal Operation		
		1	Mic Open Connection		
4	MICH_SB4		Mic High Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Supply		
3	MICH_SG4		Mic High Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to Ground		
2	MICH_SMB4		Mic High Shorted to MICBIAS.	0x0	R
		0	Normal Operation		
		1	Mic High Shorted to MICBIAS		
1	MICL_SB4		Mic Low Shorted to Supply.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Supply		
0	MICL_SG4		Mic Low Shorted to Ground.	0x0	R
		0	Normal Operation		
		1	Mic Low Shorted to Ground		

DIAGNOSTICS INTERRUPT PIN CONTROL REGISTER 1

Address: 0x15, Reset: 0x20, Name: DIAG_IRQ1

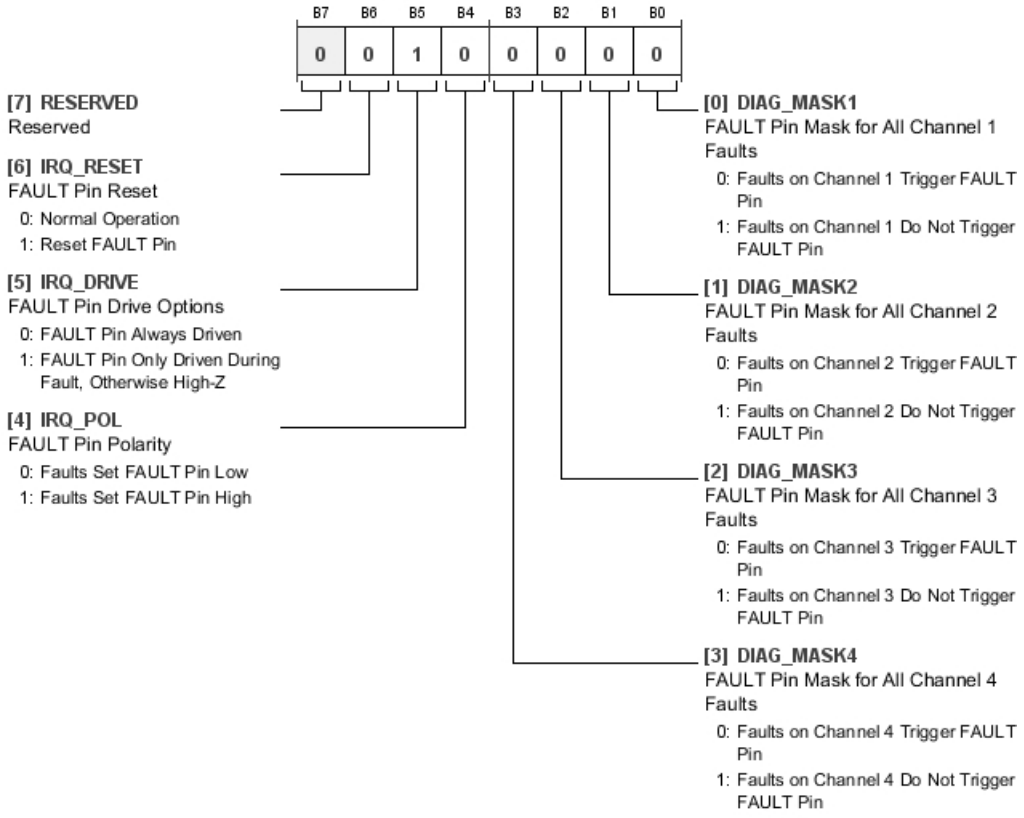


Table 46. Bit Descriptions for DIAG_IRQ1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	IRQ_RESET		FAULT Pin Reset.	0x0	RW
		0	Normal Operation		
		1	Reset FAULT Pin		
5	IRQ_DRIVE		FAULT Pin Drive Options.	0x1	RW
		0	FAULT Pin Always Driven		
		1	FAULT Pin Only Driven During Fault, Otherwise High-Z		
4	IRQ_POL		FAULT Pin Polarity.	0x0	RW
		0	Faults Set FAULT Pin Low		
		1	Faults Set FAULT Pin High		
3	DIAG_MASK4		FAULT Pin Mask for All Channel 4 Faults.	0x0	RW
		0	Faults on Channel 4 Trigger FAULT Pin		
		1	Faults on Channel 4 Do Not Trigger FAULT Pin		
2	DIAG_MASK3		FAULT Pin Mask for All Channel 3 Faults.	0x0	RW
		0	Faults on Channel 3 Trigger FAULT Pin		
		1	Faults on Channel 3 Do Not Trigger FAULT Pin		
1	DIAG_MASK2		FAULT Pin Mask for All Channel 2 Faults.	0x0	RW
		0	Faults on Channel 2 Trigger FAULT Pin		
		1	Faults on Channel 2 Do Not Trigger FAULT Pin		
0	DIAG_MASK1		FAULT Pin Mask for All Channel 1 Faults.	0x0	RW
		0	Faults on Channel 1 Trigger FAULT Pin		
		1	Faults on Channel 1 Do Not Trigger FAULT Pin		

DIAGNOSTICS INTERRUPT PIN CONTROL REGISTER 2

Address: 0x16, Reset: 0x00, Name: DIAG_IRQ2

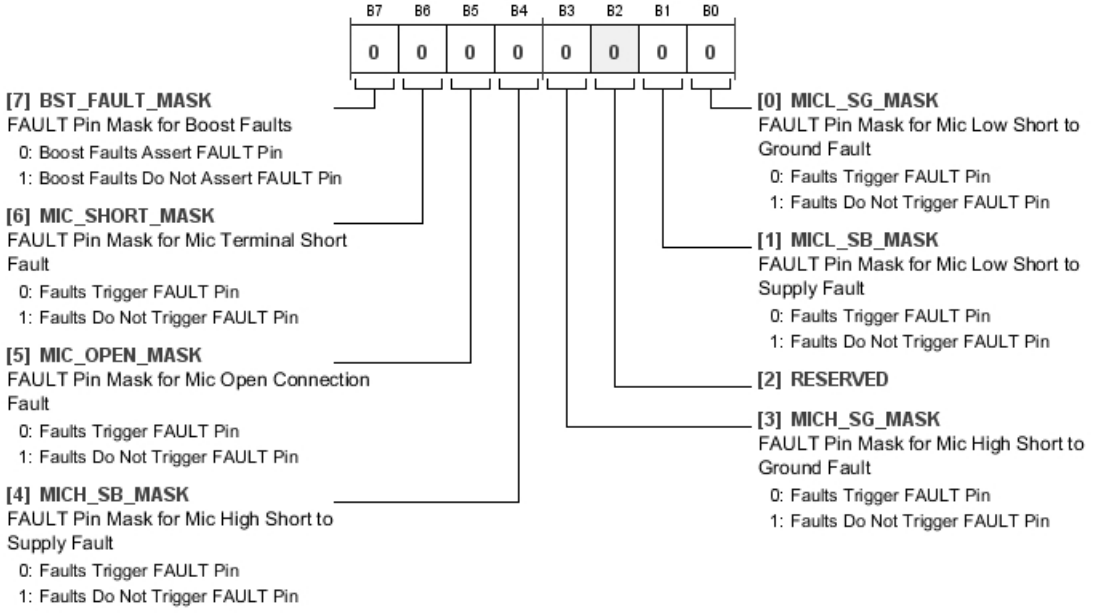


Table 47. Bit Descriptions for DIAG_IRQ2

Bits	Bit Name	Settings	Description	Reset	Access
7	BST_FAULT_MASK		FAULT Pin Mask for Boost Faults.	0x0	RW
		0	Boost Faults Assert FAULT Pin		
		1	Boost Faults Do Not Assert FAULT Pin		
6	MIC_SHORT_MASK		FAULT Pin Mask for Mic Terminal Short Fault.	0x0	RW
		0	Faults Trigger FAULT Pin		
		1	Faults Do Not Trigger FAULT Pin		
5	MIC_OPEN_MASK		FAULT Pin Mask for Mic Open Connection Fault.	0x0	RW
		0	Faults Trigger FAULT Pin		
		1	Faults Do Not Trigger FAULT Pin		
4	MICH_SB_MASK		FAULT Pin Mask for Mic High Short to Supply Fault.	0x0	RW
		0	Faults Trigger FAULT Pin		
		1	Faults Do Not Trigger FAULT Pin		
3	MICH_SG_MASK		FAULT Pin Mask for Mic High Short to Ground Fault.	0x0	RW
		0	Faults Trigger FAULT Pin		
		1	Faults Do Not Trigger FAULT Pin		
1	MICL_SB_MASK		FAULT Pin Mask for Mic Low Short to Supply Fault.	0x0	RW
		0	Faults Trigger FAULT Pin		
		1	Faults Do Not Trigger FAULT Pin		
0	MICL_SG_MASK		FAULT Pin Mask for Mic Low Short to Ground Fault.	0x0	RW
		0	Faults Trigger FAULT Pin		
		1	Faults Do Not Trigger FAULT Pin		

DIAGNOSTICS ADJUSTMENTS REGISTER 1

Address: 0x17, Reset: 0x00, Name: DIAG_ADJUST1

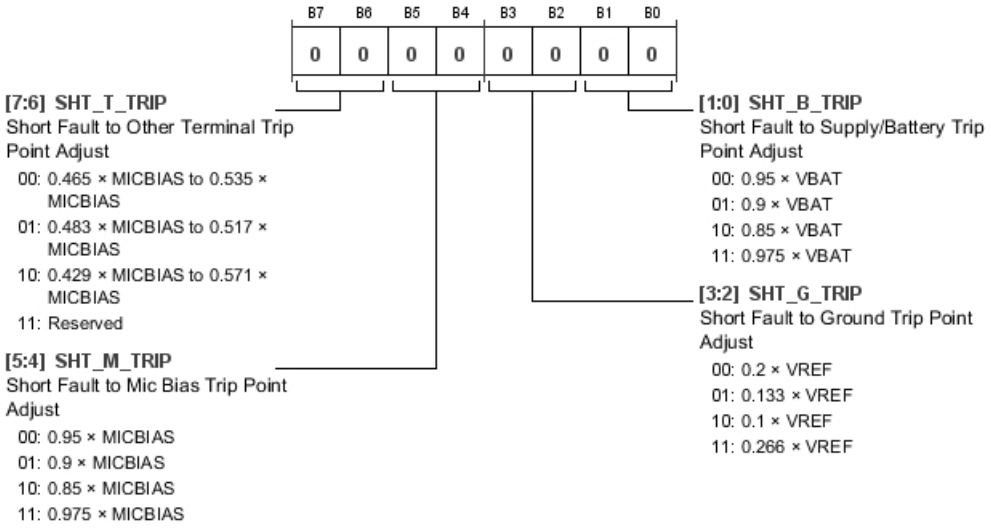


Table 48. Bit Descriptions for DIAG_ADJUST1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SHT_T_TRIP		Short Fault to Other Terminal Trip Point Adjust.	0x0	RW
		00	0.465 × MICBIAS to 0.535 × MICBIAS		
		01	0.483 × MICBIAS to 0.517 × MICBIAS		
		10	0.429 × MICBIAS to 0.571 × MICBIAS		
		11	Reserved		
[5:4]	SHT_M_TRIP		Short Fault to Mic Bias Trip Point Adjust.	0x0	RW
		00	0.95 × MICBIAS		
		01	0.9 × MICBIAS		
		10	0.85 × MICBIAS		
		11	0.975 × MICBIAS		
[3:2]	SHT_G_TRIP		Short Fault to Ground Trip Point Adjust.	0x0	RW
		00	0.2 × VREF		
		01	0.133 × VREF		
		10	0.1 × VREF		
		11	0.266 × VREF		
[1:0]	SHT_B_TRIP		Short Fault to Supply/Battery Trip Point Adjust.	0x0	RW
		00	0.95 × VBAT		
		01	0.9 × VBAT		
		10	0.85 × VBAT		
		11	0.975 × VBAT		

DIAGNOSTICS ADJUSTMENTS REGISTER 2

Address: 0x18, Reset: 0x20, Name: DIAG_ADJUST2

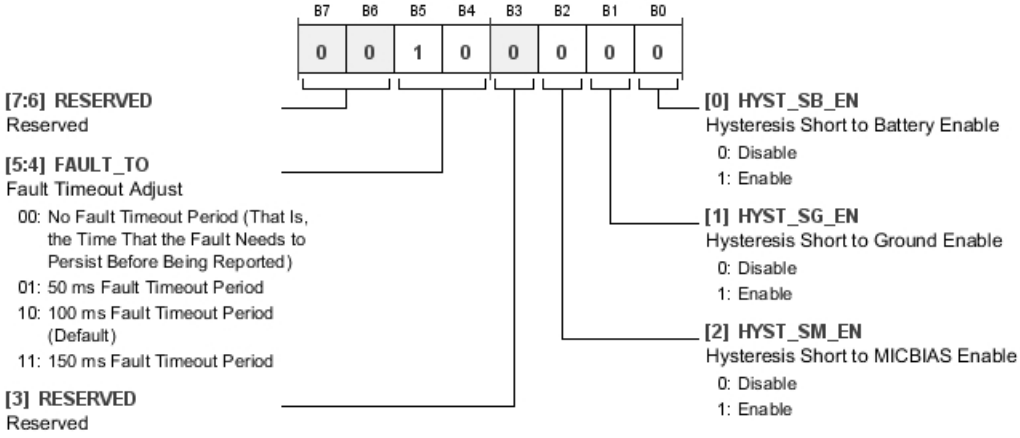


Table 49. Bit Descriptions for DIAG_ADJUST2

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
[5:4]	FAULT_TO		Fault Timeout Adjust.	0x2	RW
		00	No Fault Timeout Period (That Is, the Time That the Fault Needs to Persist Before Being Reported)		
		01	50 ms Fault Timeout Period		
		10	100 ms Fault Timeout Period (Default)		
		11	150 ms Fault Timeout Period		
3	RESERVED		Reserved.	0x0	RW
2	HYST_SM_EN		Hysteresis Short to MICBIAS Enable.	0x0	RW
		0	Disable		
		1	Enable		
1	HYST_SG_EN		Hysteresis Short to Ground Enable.	0x0	RW
		0	Disable		
		1	Enable		
0	HYST_SB_EN		Hysteresis Short to Battery Enable.	0x0	RW
		0	Disable		
		1	Enable		

ADC CLIPPING STATUS REGISTER

Address: 0x19, Reset: 0x00, Name: ASDC_CLIP

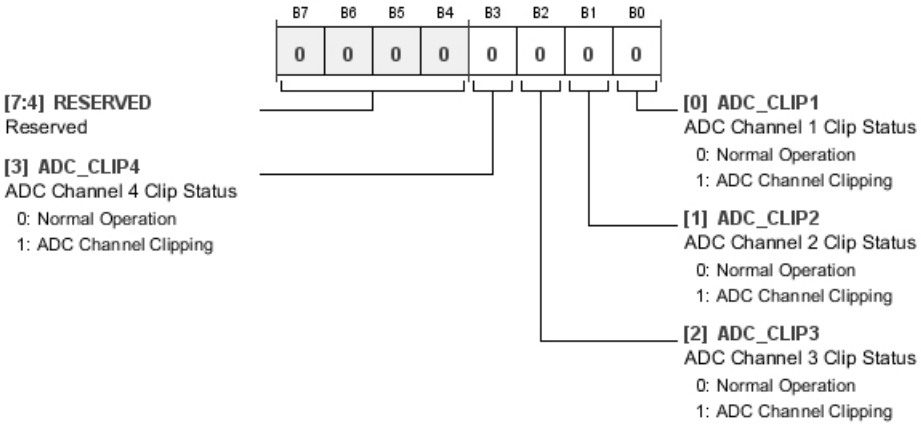


Table 50. Bit Descriptions for ASDC_CLIP

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
3	ADC_CLIP4		ADC Channel 4 Clip Status.	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		
2	ADC_CLIP3		ADC Channel 3 Clip Status.	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		
1	ADC_CLIP2		ADC Channel 2 Clip Status.	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		
0	ADC_CLIP1		ADC Channel 1 Clip Status.	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		

DIGITAL DC HIGH-PASS FILTER AND CALIBRATION REGISTER

Address: 0x1A, Reset: 0x00, Name: DC_HPF_CAL

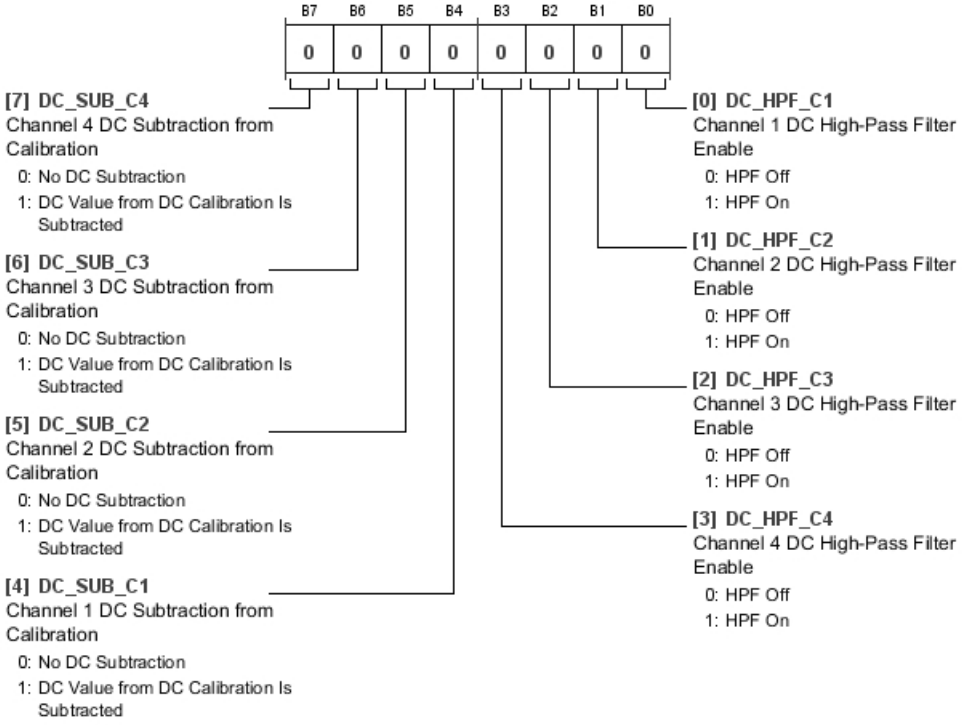
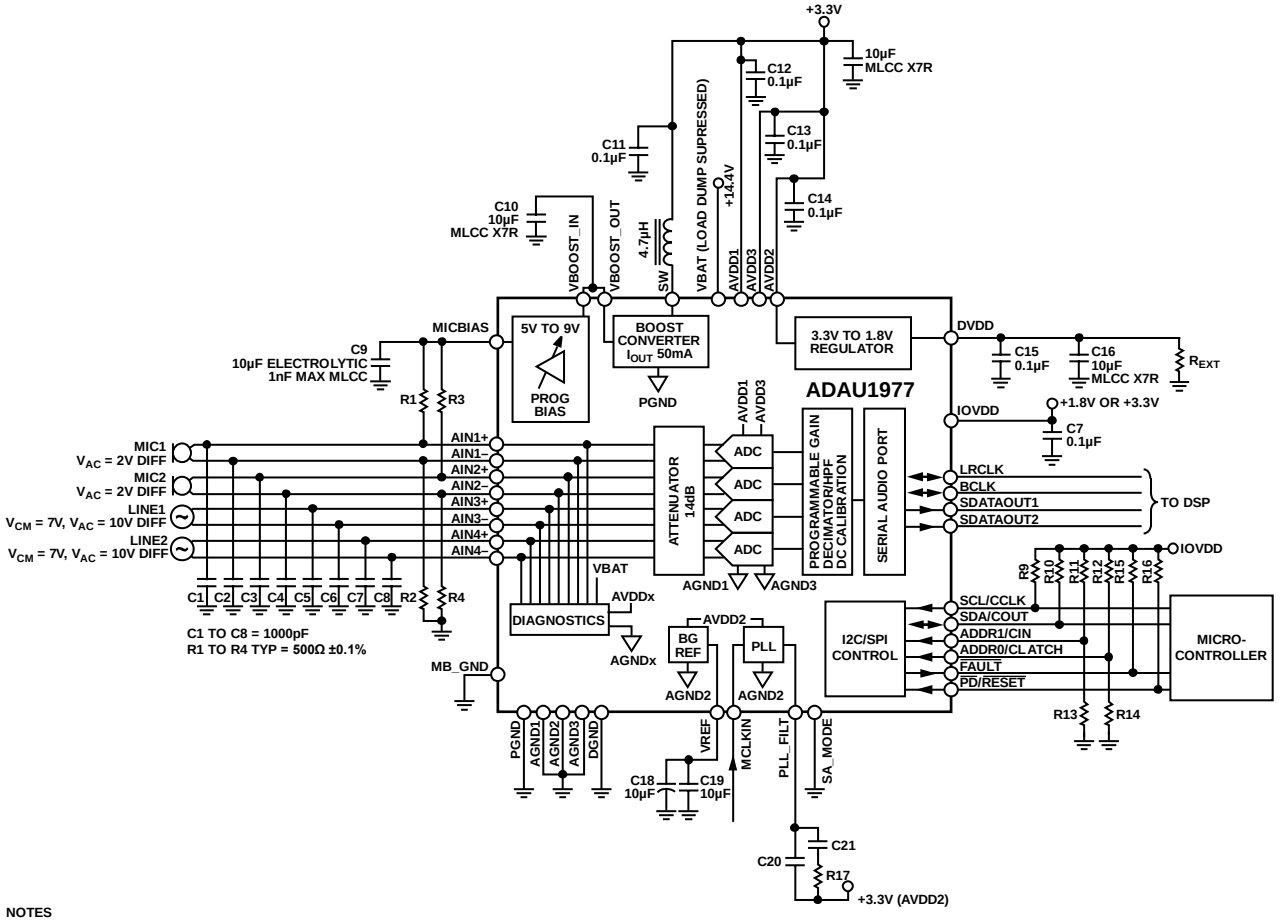


Table 51. Bit Descriptions for DC_HPF_CAL

Bits	Bit Name	Settings	Description	Reset	Access
7	DC_SUB_C4		Channel 4 DC Subtraction from Calibration.	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
6	DC_SUB_C3		Channel 3 DC Subtraction from Calibration.	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
5	DC_SUB_C2		Channel 2 DC Subtraction from Calibration.	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
4	DC_SUB_C1		Channel 1 DC Subtraction from Calibration.	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
3	DC_HPF_C4		Channel 4 DC High-Pass Filter Enable.	0x0	RW
		0	HPF Off		
		1	HPF On		
2	DC_HPF_C3		Channel 3 DC High-Pass Filter Enable.	0x0	RW
		0	HPF Off		
		1	HPF On		
1	DC_HPF_C2		Channel 2 DC High-Pass Filter Enable.	0x0	RW
		0	HPF Off		
		1	HPF On		
0	DC_HPF_C1		Channel 1 DC High-Pass Filter Enable.	0x0	RW
		0	HPF Off		
		1	HPF On		

APPLICATIONS CIRCUIT



NOTES
1. R9, R10, R15 = TYPICAL 2kΩ FOR IOVDD = 3.3V, 1kΩ FOR 1.8V.
2. R11 THROUGH R14 USED FOR SETTING THE DEVICE IN I²C MODE.
3. R16 = TYPICAL 47kΩ FOR IOVDD = 3.3V, 22kΩ FOR 1.8V.
4. PLL LOOP FILTER:

	PLL INPUT OPTION	
	LRCLK	MCLK
R17	4.87kΩ	1kΩ
C20	2200pF	390pF
C21	39nF	5600pF

5. FOR MORE INFORMATION ABOUT CALCULATING THE VALUE OF R_{EXT}, SEE THE POWER-ON RESET SEQUENCE SECTION.

10296-046

Figure 46. Typical Application Schematic—Two Microphones, Two Line Inputs, I²C and I²S Mode

OUTLINE DIMENSIONS

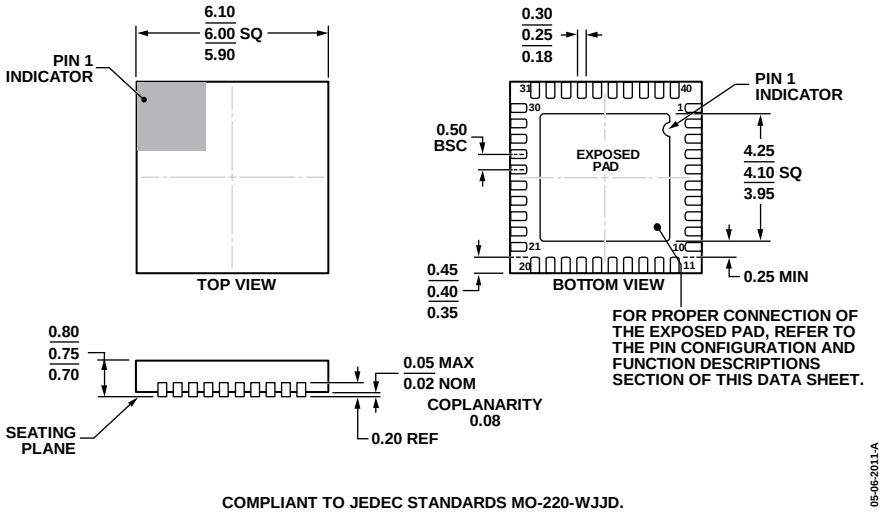


Figure 47. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADAU1977WBCPZ	–40°C to +105°C	40-Lead LFCSP_WQ	CP-40-9
ADAU1977WBCPZ-R7	–40°C to +105°C	40-Lead LFCSP_WQ, 7″ Tape and Reel	CP-40-9
ADAU1977WBCPZ-RL	–40°C to +105°C	40-Lead LFCSP_WQ, 13″ Tape and Reel	CP-40-9
EVAL-ADAU1977Z		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADAU1977WBCPZ, ADAU1977WBCPZ-R7, and ADAU1977WBCPZ-RL models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.